# Analysis and Implementation of Unipolar PWM Strategies for Three Phase Cascade Multilevel Inverter Fed Induction Motor Drive

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#### **ABSTRACT**

This paper presents unipolar pulse width modulation technique with sinusoidal sampling pulse width modulation are analyzed for three-phase five-level, seven-level, nine-level and eleven-level cascaded multi-level inverter. The unipolar PWM method offers a good opportunity for the realization of the Three-phase inverter control, it is better to use the unipolar PWM method with single carrier wave compared to two reference waves. In such case the motor harmonic losses will be considerably lower. The necessary calculations for generation of unipolar pulse width modulation strategies have presented in detail. The unipolar SPWM voltage switching scheme is selected in this paper because this method offers the advantages of effectively doubling the switching frequency of the inverter voltage. The cascaded multi level inverter fed induction motor is simulated and compared the total harmonic distroction for all level (five-level, seven-level, nine-level and elevel-level) of the inverter. Theoretical investigations were confirmed by the digital simulations using MATLAB/SIMULINK software.

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245

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#### 1. INTRODUCTION

The pulse width modulation (PWM) strategies are the most effective to control multilevel inverters. The unipolar PWM are the most preferred pwm control techniques. Even though space vector modulation (SVM) is complicated, it is the preferred method to reduce power losses by decreasing the power electronics devices switching frequency, which can be limited by pulse width modulation. The operation theory will be discussed with the aspect of Unipolar PWM [1]. In the region of high voltage and power, a high quality inverter fed ac drive is more easily obtained by the use of multi-level and in the first turn of three-level inverters. The neutral point clamped three-level inverter topology is presented. Several PWM methods for this inverter have been elaborated previously [2], [3].

The most popular method is based on the intersection of a single sinusoidal reference with N-1 triangular carriers, originally proposed by carara et al [4], [5].three alternative carrier disposition schemes are suggested, namely PD,POD,APOD.Another important topology, named Cascade H-Bridge (CHB), has fewer components to achieve the same number of output voltage levels. It is one of the most widely used topologies due to its reliability and increased capacity to operate under fault conditions in the cells [6], [7].

In this paper the Unipolar PWM strategy of five-level, seven-level, nine-level and eleven-level inverters are compared for THD. The paper mainly deals with the computation and the comparison of the motor harmonic losses of unipolar PWM solutions and with the selection of the solutions providing the best

246 □ ISSN: 2252-8814

results. Finally, the drive harmonic losses will be compared for (five-level, seven-level,nine-level and eleven-level) inverters.

#### 2. THREE-PHASE N-LEVEL CASCADED H-BRIDGE MULTI-LEVEL INVERTER

The three phase Series H-bridge inverter (SHI) or Cascaded Multi-Level Inverter (CMI) topology shown in Figure 1. by al will have broad strategy with an better harmonic performance. This strategy consists single carrier from each H-bridge cell (Where N is number of level). Single leg N-level inverter CHB inverter is shown in Figure 1. Each cell contains four active switches S1 to S4 with anti-parallel diodes D1 to D4. Each cell contains separated DC source. And each cell produced three different voltage level (+E,0,-E). The phase voltage consists of N-level inverter, the levels in phase voltage are 2N+1, here N is  $1-\phi$  inverter cells present in a phase and the number of levels in line voltage are 2M-1, where M is the number of level in phase voltage [8], [9].

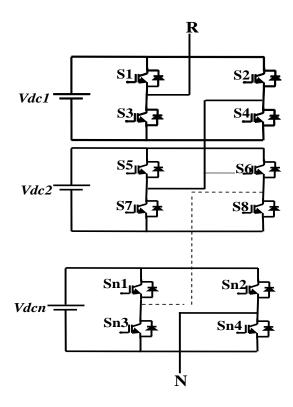


Figure 1. Single leg N-level cascaded H-bridge multilevel inverter

## 3. GENERALIZED UNIPOLAR PWM TECHNIQUE FOR CASCADED H-BRIDGE MULTI-LEVEL INVERTER

Figure 2. Illustrates the unipolar multi level modulation strategy.the modulation signals have the same frequency (fo) and amplitude (Am). The sinusoidal signals are sampled by a triangular carrier signal with frequency (fc) and amplitude (Ac) once every cycle, intersection between the sampled modulation signals and the carrier signal defines the switching instant of the PWM pulses. In order to ensure quarter wave symmetric properties of the PWM output waveform, the starting point of the modulation signals is phase shifted by one period of the carrier wave, in addition the frequency modulation ratio (mf) must also be even number [10], [11].

The unipolar PWM method offers a good opportunity for the realization of the Three-phase inverter control. In case of the five-level, seven-level, nine-level and eleven-level inverters it is better to use the unipolar PWM method with three carrier waves. In such case the motor harmonic losses will be considerably lower. The unipolar spwm voltage switching scheme is selected in this paper because this method offers the advantages of effectively doubling the switching frequency of the inverter voltage. A particular advantage of the unipolar PWM approach is that, this method reduces the harmonics in the three phase inverter.

That means, selecting unipolar PWM as switching scheme in the proposed inverter is appropriate as there is no filter at the inverter output compared to other spwm techniques.

In this scheme, the triangular carrier waveform is compared with two reference signals which are positive and negative signal. The basic idea to produce SPWM with unipolar voltage switching is shown in Figure 2. The different between the Bipolar SPWM generators is that the generator uses another comparator to compare between the inverse reference waveform—Vr . The process of comparing these two signals to produce the unipolar voltage switching signal is graphically illustrated in Figure 2. In Unipolar voltage switching the output voltage switches between 0 and Vdc, or between 0 and —Vdc. This is in contrast to the Bipolar switching strategy in which the output swings between Vdc and—Vdc. Over modulation occurs when amplitude modulation index ma is greater than unity. It causes a reduction in number of pulses in the line to line voltage waveform leading to emergence of lower order harmonics. Moreover the notch and pulse widths near the center of positive and negative half cycle tend to vanish. To complete the switching operations of the device, minimum notch and pulse widths must be maintained. When minimum width notches and pulses are dropped, there will be some transient jump of load current. The generated signals are as shown in Figure 2 and the switching pulses generated shown in Figure 3.and the output currents at the load shown in Figure 4. The modulation index is the ratio of peak magnitudes of the modulating signal Vm and the carrier signal:

$$m = \frac{Vm}{V_C} \tag{2}$$

The modulation index in SPWM technique for cascaded multilevel inverter configuration is given by:

$$m = \frac{Vm}{(N-1)Vc} \tag{3}$$

where N is number of levels. For under modulation 0 < m < 1. For over modulation m > 1.

Generally, over modulation is not desired because of the presence of the lower frequency harmonics in the output voltage and subsequent distortion in the load current [12]. Frequency modulation is the ratio of frequency of the triangular carrier signal fc to the frequency of sinusoidal reference signal fs . It controls harmonics in the output voltage.

$$mf = \frac{fc}{fs} \tag{4}$$

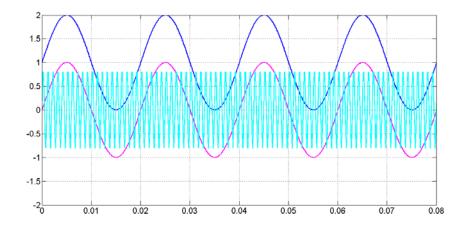


Figure 2. Unipolar PWM technique pulse generation

248 ISSN: 2252-8814

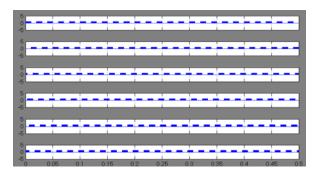


Figure 3. Switching Pulses generation using Unipolar PWM technique

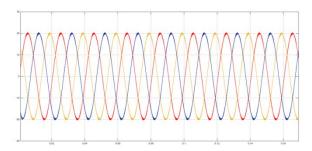


Figure 4. Output current at the load

#### SIMULATION RESULTS AND ANALYSIS

The N-level cascaded multilevel inverter fed induction motor is considered for simulation. The simulation study is carried out using MATLAB/SIMULINK. The system parameters are shown in Table 1.

Table 1. The Parameter of the Induction Motor		
Parameters	Specifications	
Input voltage	400VRMS(PhasePhase)	
Invioutou violto oo	100(Valta)	

Inverter voltage 100(Volts) 1440(RPM) Rotor speed Fundamental frequency 1200(Hz) Switching frequency 1200(Hz) 1500(RPM) Reference speed

The simulation of the cascaded multi-level inverter fed induction motor and observe the stator current,torque,speed of the induction motor and THD of the line voltage (five-level, seven-level, nine-level and eleven-level). As per the principle of unipolar pwm two reference sine and single carrier waves are compared. The generated signals are as shown in Figure 2. Which contain single carrier comparead other spwm techniques (multi carrier techniques).

## 3.1. Unipolar PWM technique applied to five-level CHBMLI

The output voltage of the inverter for line to line is about 410V when using Unipolar PWM. Here in Figure 5.one can observe the line voltages of five level inverter. Here in Figure 6. Indicates the three phase output stator currents of the load and we can observe the system is unstable from o to 0.15 sec.due to transient behavior of the system at the starting from 0.15 sec. Figure 7.indicates the torque, speed of the load of five level inverter from the figure it can be seen that the steady state operation of the system has achieved at 0.2 sec.

The total harmonic distortion of the output voltage is about 23.13%, at ma=1.5, mf=31.84. When using Unipolar PWM technique on five-level cascaded multi-level inverter shown in Figure 8.

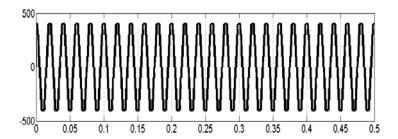


Figure 5. Proposed five-level Unipolar PWM technique (Line voltage)

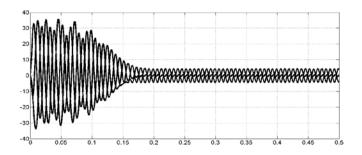


Figure 6. Output stator currents of the load (Five-level inverter)

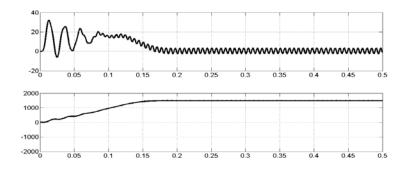


Figure 7. Output torque and speed of the load (Five-level inverter)

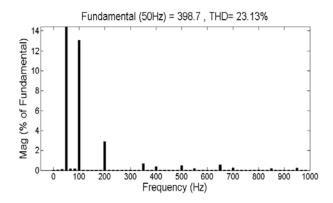


Figure 8. THD For Unipolar technique m<sub>a</sub>=1.5,m<sub>f</sub>=31.84

250 ☐ ISSN: 2252-8814

### 3.2. Unipolar PWM technique applied to seven-level CHBMLI

The output voltage of the inverter for line to line is about 410V. Here in Figure 9. One can observe the line voltages of seven level inverter using unipolar PWM technique. Here in Figure 10. Indicates the three phase output stator currents of the load and we can observe the system is unstable from 0 to 0.2 sec. Due to transient behavior of the system at the starting from 0.2 sec. Figure 1I. Indicates the torque, speed of the load of seven level inverter from the figure it can be seen that the steady state operation of the system has achieved at 0.15 sec.

Figure 12. Indicate the total harmonic distortion of the output voltage is about 15.33%, at ma=1.3, mf=31.84 when using Unipolar PWM technique on seven-level cascaded multi-level inverter.

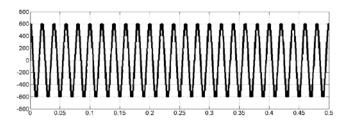


Figure 9. Proposed seven-level Unipolar PWM technique (Line voltage)

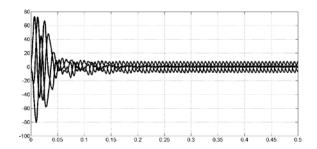


Figure 10. Output stator currents of the load (Seven-level inverter)

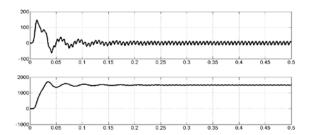


Figure 11. Output torque and speed of the load (Sevenive -level inverter)

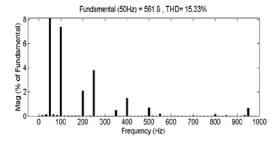


Figure 12. THD For Unipolar technique ma=1.3,mf=31.84

#### 3.3. Unipolar PWM technique applied to nine-level CHBMLI

The output voltage of the inverter for line to line is about 410V. Here in Figure 13. One can observe the line voltages of nine level inverter using unipolar PWM technique. Here in Figure 14. Indicates the three phase output stator currents of the load and we can observe the system is unstable from 0 to 0.3 sec. Due to transient behavior of the system at the starting from 0.3 sec.and Figure 15. Indicates the torque, speed of the load of nine level inverter from the figure it can be seen that the steady state operation of the system has achieved at 0.35 sec.

Figure 16. Indicate the total harmonic distortion of the output voltage is about 10.78%, at ma=1.2, mf=31.84 when using unipolar PWM technique on nine-level cascaded multi-level inverter.

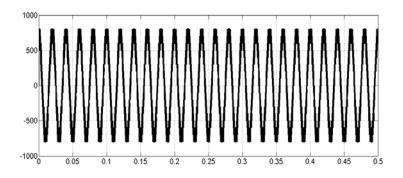


Figure 13. Proposed nine-level Unipolar PWM technique (Line voltage)

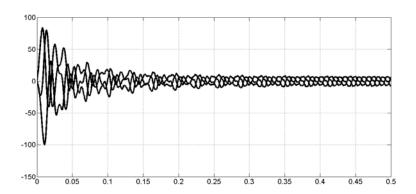


Figure 14. Output stator of the load (Nine-level inverter)

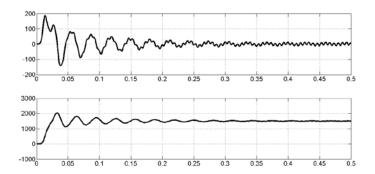


Figure 15. Output torque and speed of the load(Nine-level inverter)

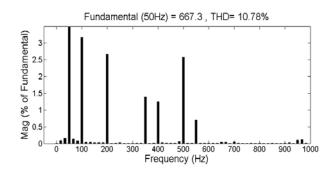


Figure 16. THD For Unipolar technique ma=1.2,mf=31.84

## 3.3. Unipolar PWM technique applied to eleven-level CHBMLI

The output voltage of the inverter for line to line is about 410V. Here in Figure 17. One can observe the line voltage of eleven level inverter using unipolar PWM technique. Here in Figure 18. Indicates the three phase output stator currents of the load and we can observe the system is unstable from 0 to 0.4 sec. Due to transient behavior of the system at the starting from 0.4 sec. Figure 19. Indicates the torque, speed of the load of eleven level inverter from the figure it can be seen that the steady state operation of the system has achieved at 0.45 sec.

Figure 20. Indicate the total harmonic distortion of the output voltage is about 10.13%, at ma=1.0, mf=31.84 when using unipolar PWM technique on eleven-level cascaded multi-level inverter.

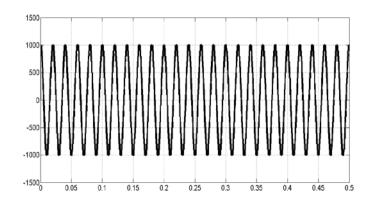


Figure 17. Proposed eleven-level Unipolar PWM technique (Line voltage)

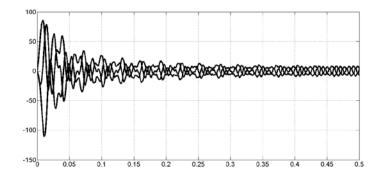


Figure 18. Output stator current of the load (Eleven-level inverter)

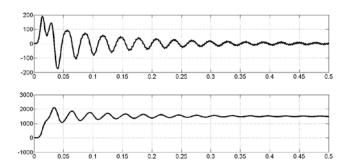


Figure 19. Output torque and speed of the load (Eleven-level inverter)

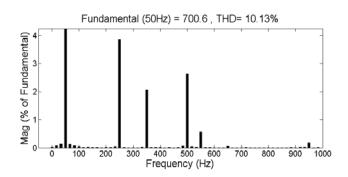


Figure 20. THD for Unipolar technique ma=1.0,mf=31.84

The total harmonic distraction waveforms obtained from the simulation results using MATLAB/SIMULINK and compared the all levels (five, seven, nine and eleven)of the cascaded multi level inverter. The comparison are made for the total harmonic distraction wave forms based on variations of parameters amplitude modulation (ma) and frequency modulation (mf).and we can observe the three phase stator currents, torque and speed of the induction motor for all levels of the inverter.the total harmonic distortion of the output voltage is about 10.13%, at ma=1.0,mf=31.84 on eleven-level cascaded multi-level inverter.The Comparison of THD analysis of a three-phase cascaded inverter fed to induction motor shown in Table 2.

Table 2. The Comparision of THD Of Five, Seven, Nine and Eleven-level Cascaded Inverter

Output Voltage Level	Techniques	%THD(V)
Five-level	Unipolar PWM	23.13
Seven-level	Unipolar PWM	15.33
Nine-level	Unipolar PWM	10.78
Eleven-level	Unipolar PWM	10.13

## 5. CONCLUSION

In this paper the Unipolar PWM technique of most proffered control strategies applied to three phase cascaded inverter are presented. The waveforms clearly depicting that almost all the five-level, seven-level, nine-level and eleven-level control strategies are functioning well in controlling the speed of the induction motor, output line voltage, stator current, speed and torque. But THD of the Unipolar PWM strategies when compared, it is obvious that eleven-level cascaded inverter is the low THD of about 10.13%.

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#### REFERENCES

[1] S.Zainal, J.Aziz, S.S.Ahmed, "Single carrier PWM scheme for cascaded multilevel voltage source inverter," Power Electronics and Drive systems, IEEE Conference (PEDC), 2003, Vol. 1, pp. 406-410.

- [2] Akira Nabae, Isao Takahashi and Hirofumi Akagi," A New Neutral-Point-Clamped Pwm Inverter", *IEEE Trans On Industry Applications*, Vol. Ia-17, No. 5. September/October 1981, Pp 518-523.
- [3] Irfan Ahmed, Vijay B. Borghate," Simplified space vector modulation technique for seven-level cascaded H-bridge inverter", IET Power Electron. 2014, Vol. 7, Iss. 3, pp. 604–613.
- [4] Carrara G.et al., "A new multilevel PWM method; A theoretical analysis", Power Electronics Specialists Conference, 1990, PESC'90 record, 21st annual IEEE, pp. 363-371.
- [5] M. Calais, L.J. Borle, V.G. Agelidis, "Analysis of multicarrier PWM methods for a single-phase five level inverter," IEEE Power Electronics Specialists Conference (PESC), 2001, Vol. 3, pp. 1351-1356.
- [6] Ravi kumar Bhukya, P. Satish kumar "Performance Analysis of Modified SVPWM Strategies for Three Phase Cascaded Multi-level Inverter fed Induction Motor Drive", international journal of power electronics and drive systems, Vol. 8, No. 2, pp. 835-843, May.2017.
- [7] J.Rodriguez, J.S.Lai, and F.Z.Peng, "Multilevel inverters: A survey of topologies, control and applications," IEEE Trans.Ind.Electron., vol.49, no.4, pp.724-738, Aug.2002.
- [8] M.Malinowski, K.Gopakumar, J.Rodriguez and A.Perez," A Survey on Cascaded Multilevel Inverters," IEEE Trans.Ind.Electron, vol.57, No.7, pp.2197-2205, July 2010.
- [9] F. Salim and N.A. Azli, "Development of an FPGABased Gate Signal Generator for a Multilevel Inverter." Proceedings of 2003 International Conference on Power Electronics and Drive Systems PED 2003, Singapore. 17-20 November 2003.
- [10] P. Palanivel, S.S. Dash "Analysis of THD and output voltage performance for cascaded multilevelinverter using carrier pulse width modulation technique" IET Power Electronics vol. 4, no. 8, pp. 951-958, 2010.
- [11] M. Satyanarayana, P. Satish Kumar, "Analysis and Design of Solar Photo Voltaic Grid Connected Inverter", *Indonesian Journal of Electrical Engineering and Informatics* (IJEEI), IAES, December 2015, Vol. 3, pp 199-208.
- [12] Ravikumar Bhukya, P.Satish kumar, Modeling, Analysis and Comparative of Down Sampling based Clamping SV PWM for Cascaded and Diode Clamped Multilevel Inverter fed Induction Motor Drive. Indonesian Journal of Electrical Engineering and Computer Science Vol. 7, No. 3, September 2017, pp. 698 ~ 707 DOI: 10.11591/ijeecs.v7.i3.pp698-707.