International Journal of Advances in Applied Sciences (IJAAS)
Vol. 10, No. 1, March 2021, pp. 79~87
ISSN: 2252-8814, DOI: 10.11591/ijaas.v10.i1.pp79-87

Second order noise shaping for data-weighted averaging technique to improve sigma-delta DAC performance

Ali Kerem Nahar[1], Ansam Subhi Jaddar[2], Hussain K. Khleaf[3], Mohmmed Jawad Mortada Mobarek[4]
[1,2,3]Department of Electrical Engineering, University of Technology, Baghdad, Iraq
[4]Najaf Gas Turbine Power Plant, Najaf, Iraq

Article Info

Article history:

Received Oct 3, 2020
Revised Dec 11, 2020
Accepted Feb 5, 2021

Keywords:

Data weighted averaging
Delta sigma
Digital-to-analog convertor
Noise shaping

ABSTRACT

In general, the noise shaping responses, a cyclic second-order response is delivered by the method of data weighted averaging (DWA) in which the output of the digital-to-analog converter (DAC) is restricted to one of two states. DWA works efficiently for rather low levels of quantizing; it begins presenting considerable difficulties when internal levels of quantizing are extended further. Though, each added bit of internal quantizing causes an exponentially increasing in power dissipation, complexity, and size of the DWA logic and the DAC. This gives a controlled second-order response accounting for the mismatch of the elements of DAC. The multi-bit DAC is made up of numerous single-bit DACs having values thereof chosen via a digital encoder. This research presents a discussion of the influence of mismatching between unit elements of the delta-sigma DAC. This results in a constrained second-order response accounting for a mismatch of DAC elements. The results of the simulation showed how the effectiveness of the DWA method in reducing band tones. Furthermore, the DWA method has proved its efficiency in solving the mismatching of DAC unit elements. The noise of the mismatching elements is enhanced by 11 dB at 0.01 with the proposed DWA, thereby enhancing the efficiency of the DAC in comparison to the efficiency of the DAC with no use of the circuit of DWA.

Corresponding Author:

Ali Kerem Nahar
Department of Electrical Engineering
University of Technology
62 University Street, Hay Al-Karada, Bahgdad, Iraq
Email: alikareemnahar79@gmail.com

1. INTRODUCTION

Delta sigma (Δ-∑) digital-to-analog converters (DAC's) and analog-to-digital converters (ADCs), together known as Δ-∑ converters of data, are common in the applications that are highly accurate with a low bandwidth, like digital audio processing. Using over-sampling, the width of the data path may be reduced from, such as (16 to1) bits. The resulting quantizing noise because of the quantization from 16 bits to 1 is formed in a way that noise is isolated outside the band of the signal. Using smaller data path simplifies designing the analog circuit, due to the fact that a data path of, one bit, for example, is the simpliest for analog design [1], [2]. For improving the efficiency of a Δ-∑ data converter, noise shaping has been utilized. Via the increase in the noise shaping order, this in-band noise performance is possible to be enhanced. In order to solve the issue using element matching, different approaches have been utilized for example, dynamic element matching in multitier noise-shaping DACs. In those approaches, the mismatches are accepted as unavoidable, with avoiding their negative via signal processing, in other words, an intelligent selecting of DACs which are utilized in converting [3].

The main reason behind using a multisite modulator is because it lowers out band noise, thereby requiring less analog circuitry for filtering. Some of the other advantages are that the modulator has higher stability, and requires smaller order and a higher factor of gain, in second advantage lies in the fact that its in-band noise is less, in addition to having smaller sensitivity of output jitter due to the fact that the steps are smaller in the output. Linear performance could only be accomplished in the case where the steps between neighboring levels of the output of every DAC have highly similar magnitudes. Which, thus, needs a matching accuracy, which is on the order of the wanted accuracy of the general converting of the data, which is typically beyond the practical bounds of existing technology of manufacturing [3], [4]. For the sake of solving the issue with element matching, a wide range of approaches has been used, like the dynamic element matching in multisite noise-shaping DACs. In those methods, the mismatches are taken as unavoidable, with the negative impacts they have on being avoided via signal processing, for example, an intelligent selection of the DACs, which are utilized in converting [5].

High-resolution digital-to-analog converters (DACs) are extensively utilized for direct digital synthesis, random wave-form generation, and video signal processing. The fundamental condition of DACs for those applications is having good linearity, implying small output error and high spectral purity. For maintaining efficient linearity, trimming and calibration has been utilized for directly decreasing mismatching of elements which produce high spurious-free dynamic range (SFDR) and small maximal output error. Another approach which is referred to as dynamic element matching (DEM) has been efficiently applied for the reduction of the correlation of DAC noise to the input signal to achieve high SFDRs. Randomization, which is a DEM technique, which is typically utilized for Nyquist-rate DACs for spreading the harmonics in a form of white noise over the output spectrum. However, the possible maximal output errors of randomizing remain large due to the fact that the elements are arbitrarily chosen [6]. The digital encoder performs DEM on an input data value. The stream of selection is accomplished in a way that the DAC element mismatch noise response is shaped. The outputs are summed at a summing junction and after that filtered by a low pass filter [3].

The DEM schemes are implemented by unitary elements steering DACs. The way the elements are selected gives the name of the algorithm, and this result in a given characteristic of dynamic matching. Some of the most important are random averaging (RA), clocked averaging (CLA), individual level averaging (ILA), and DWA [7]. One of the simplest DEM schemes is the DWA, which selects the unitary elements cyclically. The main characteristic of the DWA is the capability to shape the spectrum of the mismatch error as a first order high-pass filter [8]. Utilizing a segmented feedback path with fine and coarse signals for the reduction of the complexity of DWA for modulators that include large internal quantizes. On the other hand, it arises other issues. Mathematical analyzing of the issues that are concerned with the segmentation of the digital word in the feedback path of the Σ-Δ ADC will be presented, in addition to a possible solution which utilizes frequency-shapes this mismatch error. A possible circuit design for the approach of frequency shaping will be extensively presented.

The results of the mathematical analysis and behavioral simulation will also be presented [8]. An innovative approach for noise shaping and a method for dual polarity calibration that is useful for successive approximation register type ADC. Noise with the addition of a switched capacitor is moved to higher frequencies with the noise shaping. Dual-polarity, digital calibration with minimal circuit overhead overcame the mismatching of the SAR capacitor collection. In a 0.5 μm standard CMOS system, a proof-of - concept prototype SAR-ADC with the use of the presented approaches has been developed [9]. Thus, of the extensive study on the model of the SAR and because of the dominance of the procedure of the CMOS, the SAR-ADC is aggressively extending to each of the high frequency domain of a number of 10 of MHz and high resolution in the order of 12-16 bits [10], [11]. Though, those efficiency enhancements typically coincide with the cost of increased complexity of the design or the power/area utilization. Numerous designers of applications of low power, adopting the model of SAR-ADC, keep trying to come up with solutions that might maximize the resolution of ADC with no need to sacrifice its simplicity and the power/area consumption. In this study, a new noise shaping approach is presented, which may be easily added to an existing model of SAR-ADC, in addition to a dual-polarity, digital calibration approach, compensating the capacitor mismatching with minimum circuit burdens [12].

2. DESIGN AND BEHAVIORAL MODELING

A block diagram of a DAC using the approaches of noise shaping of the existing disclosure of feed forward paths in front of the quantize in Figure 1, an adder circuit is important to realize all feed forward signals added together, creating complications for the full feed forward Δ-Σ modulators. The DAC Δ-Σ modulator and the DEM circuit are and an analog low-pass filter digital circuits. Each block of the Δ-Σ DAC is carefully designed and modeled with regard to signal-to-noise ratio (SNR), power consumption, and area [13].

The quantizing noise elements and the DAC noise outside of the band response of the signal for the Δ-Σ signal modulator output in Figure 2(a) will be eliminated by the filter but a great deal of the DAC noise will be in band. Utilizing the approaches of noise-shaping DEM produces DAC noise pushing the DAC noise outside the band of the signal as depicted in Figure 2(b); and the response of a noise-shape multi-bit DAC shown in Figure 2(c).

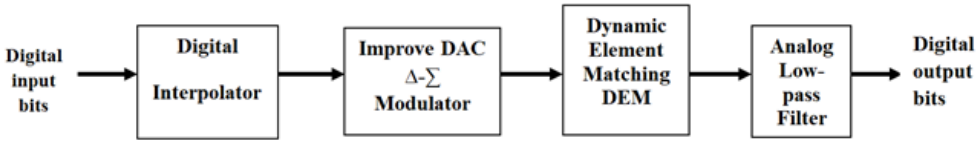


Figure 1. The digital-to-analog converter block diagram, which is utilized a multi-bit DAC with noise shaping

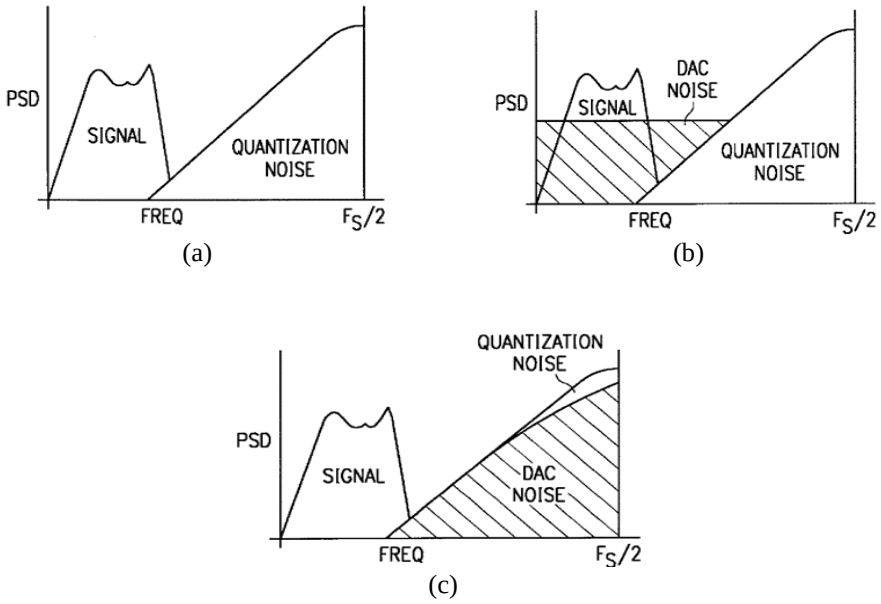


Figure 2. Usual power spectral densities at the DAC output, (a) output of the Δ-∑ signal modulator, (b) without DEM, and (c) with DEM algorithm

2.1. Design and model for the second-order improving DAC Δ-Σ modulators

In the second order system, there will be second order filters function as Mismatch-shaping transfer function (Mtf) for noise that determination as (1).

$$Mtf = (1 - z^{-1})^2 = (1 - 2z^{-1} + z^{-2}) \quad (1)$$

This is the representation of the frequency domain while, in the time domain the noise caused by the DAC is denoted for the n'th conversion in (2).

$$k(n) = K_2(n) - 2K_1(n) + K_0(n) \quad (2)$$

When, $K_1(n) = K_2(n-1)\ and\ K_1(n) = K_0(n-1)$. Figure 3 illustrates the suggested model of second-order DAC Δ-Σ modulators. It's a 3-bit second order model with a topology of single-loop single-DAC-feedback. For getting higher SNDR with low-power dissipation show, there are similar structures with 2 integrators, DAC and ADC, but with differing signal paths. The input and output of the proposed second-order DAC Δ-Σ modulator that is depicted in Figure 3 may be represented in (3).

$$Y(z) = X(z) + \alpha\left((1 - z^{-1})^2\, N(z)\right) \quad (3)$$

Where, *X(z)* denotes the input signal, $Y(z)$ denotes the output signal, *N(z)* denotes quantization noise of the modulator and $\alpha = (\frac{A_0-1}{A_0}) \cong 1$.

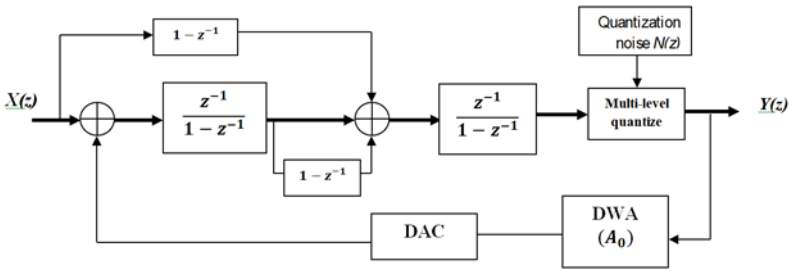


Figure 3. Proposed second-order DAC Δ-Σ modulator

2.2. Model for DEM

Multi-bits quantize in the modulator boosts signal-to-noise-ratio and eliminate the pressure of the analog low-pass filter; however, the mismatching in the unit element in the multi-bits DAC sharply diminishes the SNDR. The effect of unit element mismatch can be reduced using DWA algorithm. Though, the data weighted average mismatch shaping is only tailored to achieve first-order error filtering, because it is based on the averaging of errors [4]. A general strategy, that is vector-based mismatch shaping (VBMS), achieves second-order spectral shaping [13].

Due to the error of DAC unit capacitor, non-ideal of sigma delta modulator increase noise floor. The DEM method eliminates this noise floor and rearranges the unit capacitor. If the thermometer code selects the same unit capacitor, the SNR of the sigma delta modulator is decreased. So, preventing the selection the same capacitance and decreasing the average error, the sigma delta modulator with DWA algorithms randomize the unit capacitor. However, if the clock frequency of sigma delta modulator increases, the feedback delay time of thermometer code must quicken. If the sigma delta modulator operates clock frequency of 63.4 MHz with 2.1 MHz signal band about 27 times. Figure 4 is the proposed DWA with new block diagram and timing diagrams. Given that the order of mismatch shaping determines the slope of the noise floor, 40 dB/decade for second order VBMS and 20 dB/decade for 1st-order shaping, the second order VBMS is adopted to ensure the insensitivity of the DAC Σ-Δ to the unit element mismatch [14].

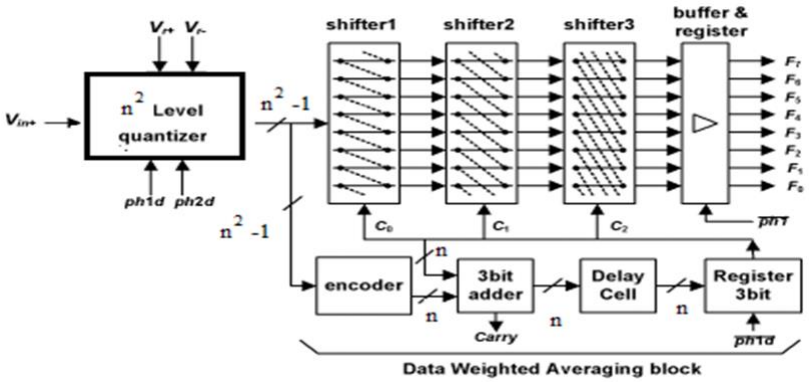


Figure 4. Block diagram of proposed DWA structure

2.3. Model for analog low-pass filter

The DAC Δ-Σ modulators are followed by an analog low-pass filter to shade the quantized noise out of the band and to smooth the output wave. The order of the analog low-pass filter must be no less than the order of the modulator in general [15], [16]; however, a high order of the analog low-pass filters indicates more OTAs and much power. Owing to the 1storder filter of the DAC Δ-Σ, the order of the analog low-pass filter is

shifted from three to two to conserve power. In addition, the 2nd-order Chebyshev Sallen-Key RC low-pass filter [17] to filter out high frequency noise is selected for its high attenuation characteristics in the transition zone.

Filter design and analysis is a helpful MATLAB tool used to design and model the analog low-pass filter [18]. Furthermore, the OTA requirement for GBW and the value of the resistor and capacitance can be obtained using the filter-pro desktop tool [19] from Texas Instruments. Proposed rapid machine learning, which is a quasi-algorithm for all multi-game machines that works on negligible facts about the online learning backend network clarification. Suggested model for algorithms other than used from the perspective of orthogonal beam, location recording, and co-site condition [20]. The overall system can be protected from voltage instability, reactive loads can be reduced, or additional reactive energy may be added to reach the voltage breakdown point [21], [22]. Flexible AC transmission devices (FACTS) make this system flexible and it is possible to prevent voltage instability with a flexible and fast control method.

3. PROPOSED DWA WITH IMPROVING DAC Δ-Σ MODULATOR BY APPLIED THE CONVERSION ALGORITHM

The proposed DWA with improving DAC Δ-Σ is desired for its high-precision time constant, low power consumption, and efficient linearity due to the well-matched metal insulation metal capacitance. It's a multi-bit second order model represented by a single-DAC-feedback, single-loop topology. Suggested modulator is about the following properties, firstly, a single amplifier saving.

In addition, a filter that has lower-order loop and multi-bit structure that second order loop filter is responsible for the reduction of the complexity of the power dissipation and the analog circuit. In addition to that, with a topology of one DAC-feedback and single-loop, the analog circuit complexity and DAC linearizing in the modulator of the Δ-Σ is diminished, and modulator is of a considerably less sensitivity to the finite gains of Dc of the amplifiers. They're more appropriate for low power dissipation. As shown in Figure 5, DAC input codes of the converting of value "1" is, by knowing that the preceding pointer k_1 equals "2" and is equal to "1." Via the insertion of the parameters of the noise in relation with the pointers, the noise equation drive is represented by (1).

$$CTRL = k_2 - 2\,k_1 + k_0 \quad (4)$$

Where, CTRL is represented as a scalar value of the summation of the eight components *CTRL(i)* the final DAC component control values and is equal to the result of the modulator, which is equal to 2, after that, a minimum of two components has to be chosen or turned on or the entire summation of the components have to be equal to 2 as an example. It's of importance considering that the previously pointed out discussion is in accordance with a system of second order. Which might easily be applied to a shaping system of a 1st order noise, CTRL=$k_1 - k_0$.

The flowchart for implementing the approach of component matching is shown in Figure 6. The program has been started at a 1st block and after that continues to a block of the function. Then, $k_1(i)$ pointer from the preceding converting is chosen as $k_0(i)$ of the existing conversion. After that, the program continues to a block of the function in which the pointer of the $k_2(i)$ is chosen from the preceding converting and replaced as the pointer of the $k_1(i)$ for the ongoing cycle of converting. After that, the program proceeds to a function block in which the k_2 is set.

In this algorithm, a midway $k_2(i)$by $I\{\,k_2(i)\}$ is determined. Which is identified with the requirement that the signal of the $CTRL(i)$ is"$0, 0, 0, 0, 0, 0, 0, 0$". As a result, the following correlation would exist for the midway pointers:

$$I\{\,k_2(i)\} = 0 + 2\,k_1(i) - k_0(i) \quad (5)$$

so, the value of $I\{\,k_2(i)\}$ is simply characterized based on $k_1(i)$ and $k_0(i)$. After this midway $k_2(i)$ The value will be determined, the determination of the program flows to a function block, where in, the step of the distribution of "1" component values for the desired CTRL value will be accomplished in a way that distributed to the smallest $I\{\,k_2(i)\}$ value positions.

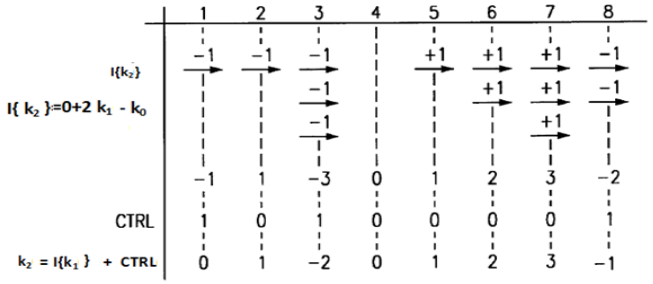


Figure 5. A diagram that illustrates selecting the DACs for a second order system

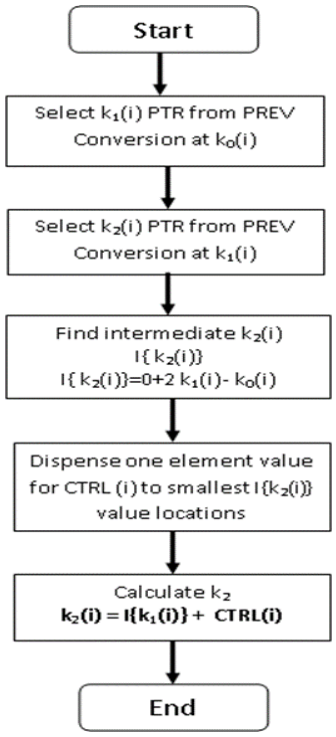


Figure 6. Flow chart of implementing the conversion algorithm

4. RESULTS AND ANALYSIS

The proposed second order DWA Circuit is used in Multi-bit DAC circuit, the DAC is composed of (1 to 10) unit elements. The behavioral simulation results are shown in Table 1 listed the factors based the proposed second order performance of the DAC modulator. The output power spectral density is presented in Figure 7. Figure 8(a) present the result of a simulation for multi-bit DAC with 0.02-unit element mismatch without using proposed DWA. Figure 8(b), at first, the frequency response is second order noise shaped and after that, flattens out over a frequency of about 500 MHz and, for this reason, the performance of the in-band noise is more efficient than the case of conventional approaches.

Table 1. Factors of the DAC Σ-Δ modulator

The factor	Value
Voltage supply	1.9 V
Bandwidth	220 kHz
Power consumption	30 mW
Switch noise	63 μV
Finite dc gain	120 dB
Finite slew rate	50 V/μs
Capacitor ratio error	5%

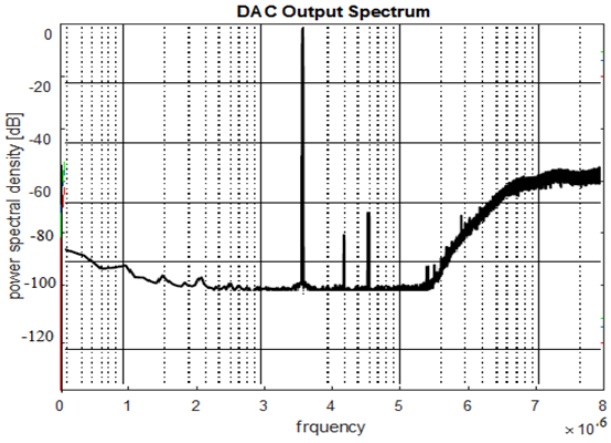
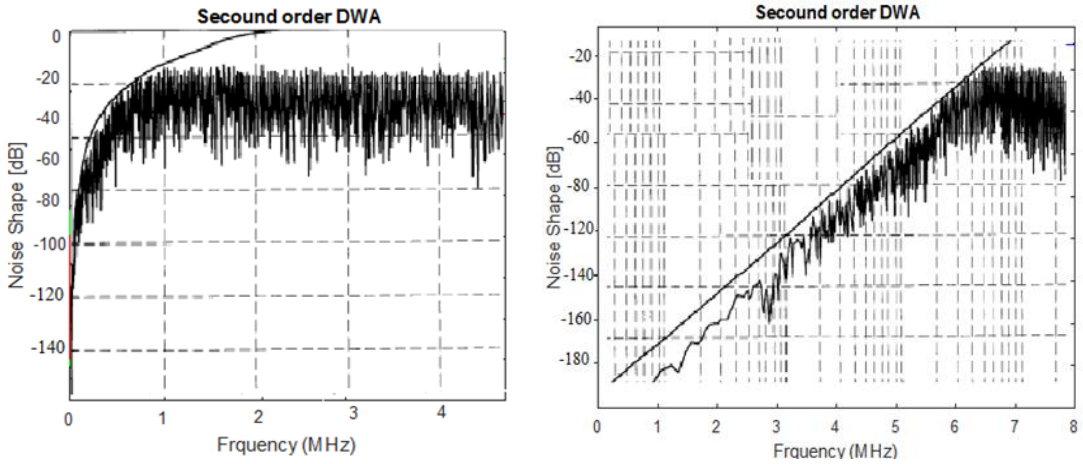


Figure 7. Simulated the output PSD of the DACs for a second order system



(a) (b)

Figure 8. Simulated for the constrained second order DWA method: (a) The result of a simulation for multi-bit DAC with 0.02-unit; and (b) The frequency response is second order noise shaped

Figure 9 illustrates the output spectrum of an improved DAC Δ-Σ modulator in Figure 7, which includes a non-linear amplifier structure with harmonic distortions. It's obvious that the gain nonlinearities of amplifiers result in considerable harmonic distortions and it is apparent in the outcome of the improved DAC Δ-Σ modulator. Compare with Figure 8, identical non-linear gain coefficients have been utilized, however, it's apparent that in this proposal of the improved DAC Δ-Σ modulator, the harmonic distortion is considerably repressed.

The behavioral simulation results are depicted in Table 2. For a level of -3 dB of the full range, and a frequency of 3 MHz with a frequency of sampling of 80 MHz input sine wave signal, the suggested improve DAC Δ-Σ boosts the SFDR by 92 dB and SNDR by 85 dB. Given that nearly all DAC Δ-Σ are for audio application, few similar DAC Δ-Σ have been reported. Comparisons of the DAC Δ-Σ between this work and other similar literature [10], [16] are listed in Table 2. Power discussed in [10] excludes the digital Δ-Σ modulator which is implemented off chip in the FPGA. FOM [18] is defined as shown in (6) for evaluating its performance and the smaller the value of FOM, the better the performance. Compared with other published DAC Δ-Σ, the proposed improve DAC Δ-Σ parades good performance in terms of FOM.

$$FOM(pJ/step) = \frac{P(mW)}{2xBWx2^{(SNDR-1.76)/6.02}} \quad (6)$$

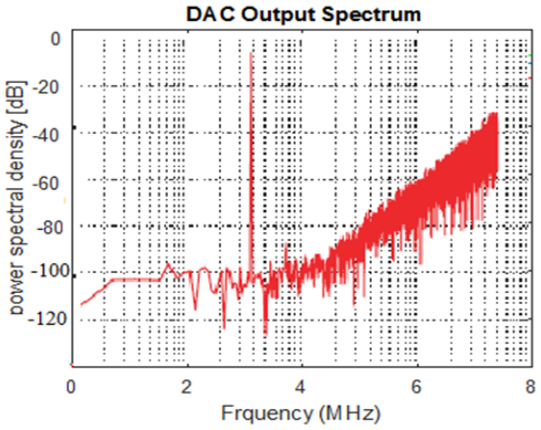


Figure 9. A depiction of the simulated output power spectrum of a suggested second order performance DAC Δ-Σ modulator

Table 2. The Comparisons of DAC Σ-Δ modulator

Factors	Ref. [11]	Ref. [23]	This work
Process	0.18 µm	0.18 µm	0.18 µm
Supply	1.2 V	1.8V	1.9 V
Power	22 mW	27 mW	30 mW
BW	312.5 KHz	200 KHz	220 kHz
SFDR	63 dB	83 dB	92 dB
SNDR	61 dB	78dB	85 dB
FOM	38 pJ/step	10 pJ/step	4 pJ/step

5. CONCLUSION

In a multi-bit implementation of the traditional DAC Δ-Σ modulators, the switched-capacitor adder has been utilized and a weighted summation amplifier is needed prior to the quantizers, which result in increasing complexity of the circuits, larger chip area, and additional dissipation of power. Some of the ideas were suggested for solving this issue. Nonetheless, they required a distributed DAC-feedback or high-order loop filter; considerably increasing the analog circuit complexity of implementing the modulator. We have proposed here improving ADC Δ-Σ modulator architecture. It is improving DAC-feedback, second order DAC Δ-Σ modulator with no extra amplifiers. The complexity of the circuit is diminished and it's better suited for low-power applications.

ACKNOWLEDGEMENTS

Thanks, and appreciation to everyone who contributed to this research, and thanks and appreciation to the Department of Electrical Engineering and the University of Technology for their support for scientific publishing and support for scientific research with all capabilities, and we also do not forget to thank all the authors.

REFERENCES

[1] Si-Nai Kim, "A 6-bit 3.3GS/s current-steering DAC with stacked unit cell structure," *Journal of Semiconductor Technology and Science*, vol. 12, no. 3, pp. 270-277, Sep 2012.

[2] Binheeim Kim, "A 40fJ/c-s 1 V 10 bit SARADC with dual sampling capacitive DAC topology," *Journal of Semiconductor Technology and Science*, vol. 11, no. 1, pp. 23-32, Mar. 2011.

[3] Ali K. Nahar, "Data weighted averaging (DWA) technique with 1st order noise-shaping to improve 6-bit digital-to-analog convertor (DAC) performance," *Journal of Babylon University/Engineering Sciences*, vol. 21, no. 5, Apr. 2013.

[4] Yongjian Tang, *et al*., "A 14 bit 200 MS/s DAC With SFDR >78 dBc, IM3 < -83 dBc and NSD < -163 dBm/Hz across the whole nyquist band enabled by dynamic-mismatch mapping," *IEEE Journal of Solid-State Circuits*, vol. 46, no. 6, pp. 1371-1381, 2011.

[5] K. Nguyen, A. Bandyopadhyay, B. Adams, et al, "A 108 dB SNR, 1.1 mW oversampling audio DAC with a three-level DEM Technique," *IEEE Journal of Solid-State Circuits*, vol.43, no. 12, pp. 2592-2600, Dec. 2008.

[6] I. Myderrizi, A. Zeki. "Current-steering digital-to-analog converters: functional specifications, design basics, and behavioral modeling," *IEEE Antennas and Propagation Magazine*, vol. 52, no. 4, pp. 197-208, Aug. 2010.
[7] E. N. Aghdam, P. Benabes, J. Abbasszadeh, "Completely first order and tone free partitioned data weighted averaging technique used in a multibit delta sigma modulator," *IEEE 19th European Conference on Circuit Theory and Design (ECCDT'09)*, 2009.
[8] A. K. Nahar, M. M. Ezzaldean, S. A. Gitaffa, H. K. Khleaf, "OFDM channel estimation based on novel local search particle swarm optimization algorithm," *Review of Information Engineering and Applications*, vol. 5, no. 2, pp. 11-21, Apr. 2017.
[9] H. K. Khleaf, A. K. Nahar, A. S. Jabbar, "Intelligent control of DC-DC converter based on PID-neural network," *International Journal of Power Electronics and Drive Systems*, vol. 10, no. 4, pp. 2254-2262, 2019.
[10] Liao Lu, Sun Ying, Han Yan, *et al*., "A 65-nm low-power high-linearity ΣΔ ADC for audio applications," *Science China (Information Sciences)*, vol. 57, pp. 201-207, 2014.
[11] X. Y. Ding, *et al*., "A CMOS oversampled closed-loop DAC with embedded filtering," *Proceedings Of the 2013 Ieee Asian Solid-State Circuits Conference*, 2013.
[12] P. Malcovati, *et al.*, "Behavioral modeling of switched–capacitor sigma–delta modulators," *IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications*, vol. 50, no. 3, pp. 352–364, Mar. 2003.
[13] M. N. Mohammed, *et al*., "Peak-to-average power ratio reduction based on optimized phase shift technique," *2017 17th International Symposium on Communications and Information Technologies (ISCIT), Cairns, QLD*, 2017.
[14] S. I. Na, *et al.*, "Estimating non-ideal effects within a top-down methodology for the design of continuous-time delta-sigma modulators," *Journal of Semiconductor Technology and Science*, vol.16, no. 3, pp. 319-329, 2016.
[15] S. Jaykar, P. Palsodkar, P. Dakhole, "Modeling of sigma-delta modulator non-idealities in MATLAB/ SIMULINK," *Communication Systems and Network Technologies (CSNT)*, pp. 525-530, Jun. 2011.
[16] E. Alothali, H. Alashwal, S. Harous, "Data stream mining techniques: a review," *TELKOMNIKA Telecommunication Computing Electronics and Control*, vol. 17, no. 2, pp. 728-737, Apr. 2019.
[17] M. S. Abdul Aziz, *et al*., "The design and evaluation of DACADE visual tool: theoretical implications," *Bulletin of Electrical Engineering and Informatics*, vol. 7, no. 1, pp. 90-95, Mar. 2018.
[18] Tony Chan Carusone, *et al*., "Analog integrated circuit design," *John Wiley & Sons, Inc*, 2011.
[19] P. M. Chopp, "Analysis of clock–jitter effects in continuous–time ΔΣ modulators using discrete–time models," *IEEE Trans. Circuits Syst. I*, vol. 56, no. 6, pp. 1134-1145, 2009.
[20] W. Shafik, *et al*., "A 3-dimensional fast machine learning algorithm for mobile unmanned aerial vehicle base stations," *International Journal of Advances in Applied Sciences (IJAAS)*, vol. 10, no. 1, 2020.
[21] R. Jena, *et al.*, "Voltage stability assessment using TCSC and SVC based FACTS controllers," *International Journal of Advances in Applied Sciences (IJAAS)*, vol. 10, no. 1, 2020.
[22] Muhammad Ayaz, "Comparative study of indoor navigation systems for autonomous flight," *TELKOMNIKA Telecommunication Computing Electronics and Control*, vol. 16, no. 1, pp. 118-128, Feb. 2018.
[23] Y. Chen, *et al*., "Modeling of a 200 KHz bandwidth low-pass switch-capacitor sigma-delta DAC with a raised spur-free modulator," *Journal Of Semiconductor Technology And Science*, vol. 17, no. 5, 2017.