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A novel fuzzy-logic controller-MDsUPQC topology for power quality improvement in multi-feeder distribution system

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ABSTRACT

In the current situation, the significant usage of massive non-linear functioned power electronic loads has been increased in domestic and industrial applications. The main problem of power-quality (PQ) deterioration in both voltage quality and current quality from nominal values and also damaging the single/multi feeder distribution systems. The major contribution is to alleviate the PQ issues by employing novel multi-devices unified power-quality conditioner (MDsUPQC) topology in a multi-feeder distribution system. This MDsUPQC comprises multiple voltage source inverter (VSI) devices connected with a common direct current-link (DC-link) capacitor which is controlled by a proportional-integral (PI) controller. However, this controller has some technical issues that are not suited for the regulation of common DC voltage at the desired level because of improper selection of gain values. The contribution of this work is proposing an intelligent fuzzy-logic (FL) DC-link controller-driven MDsUPQC device which evidences the intelligent knowledge base for better regulation of PQ issues. The technique and performance of the suggested strategy for PQ improvement, load sharing between feeders, and simulation results are presented with comparative analysis utilizing the MATLAB/Simulink software tool.

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1. INTRODUCTION

Power-quality (PQ) issues in the power distribution network are identified based on multiple circumstances that occur in sensitive load equipment and cause loss of capacity and production [1], [2]. PQ identification approaches that are viable must be used to recognize the type of PQ issue impacting the distribution network and monitoring system requirements with sophisticated monitoring techniques [3]. The problem statement of this work is to mitigate multiple PQ issues encountered in distribution systems such as harmonic current distortions, voltage harmonics, voltage sag-swells, unbalanced voltage, voltage flicker, voltage interruptions, and frequency deviations.

In this view, various electrical engineers and researchers are compelled to create sophisticated PQ improvement techniques known as customized power compensation (CPC) technology [4]. Hossain *et al*. [5] showed a few feasible scenarios on series/shunt-connected compensation devices for enhanced PQ features are presented. This CPC equipment uses custom-power devices (CPDs) to compensate for both current

and/or voltage-allied PQ issues, resulting in a multi-feeder system that is sinusoidal, linear, fundamental, and balanced [6]. The multi-feeder CPDs are classified based on specific issues such as interline-dynamic voltage restorer (IDVR) [7], and interline power-flow controller (IPFC) [8]–[10]. These compensation tools functioned independently to mitigate either voltage or current-allied PQ issues [11], [12]. The main contribution of this work is, developing the novel multi-devices unified power-quality conditioner (MDsUPQC) for mitigation of both voltage and current-related PQ issues in a multi-feeder distribution system. Furthermore, it may transfer real-time reactive energy between feeders and ensure continuous power supply to loads throughout power outages.

The proposed MDsUPQC device is made up of numerous voltage source inverters (VSIs) coupled in a shunt-series fashion and driven by a typical direct current (DC) capacitor with the appropriate voltage level. By utilizing viable reference signal extracting approaches, the proposed MDsUPQC minimizes both load and source-side PQ concerns in a three-phase multi-feeder distribution system. The suggested MDsUPQC device approach necessitates well-functioning control systems to extract reference voltage and current signals by detecting supply voltage and non-linear load currents. In general, such as the synchronous reference frame (SRF) control theory [13] was used to extract reference voltage from the series VSI-1,3 of the MDsUPQC. Also, the instantaneous real-power (IRP) control theory [14] collects the reference current from the shunt-VSI-2 of the MDsUPQC device. The direct current-link (DC-link) control of shunt-connected VSI-2 utilizes the proportional-integral (PI) controller is considered as the second problem, which is not suited for regulation of DC-link voltage at the desired level because of improper selection of gain values. The contribution of this work is proposing an intelligent fuzzy-logic (FL) DC-link controller driven MDsUPQC device which evidences the intelligent knowledge base for better regulation of PQ issues. The technique and performance of the suggested strategy for PQ improvement, load sharing between feeders, and simulation results are presented with comparative analysis utilising the MATLAB/Simulink software tool.

2. PROPOSED CONCEPT

The proposed MDsUPQC is made up of three VSI elements: one shunt-linked VSI-2 architecture to alleviate all current issues in feeder-2 and two series-VSI 1,3 elements to alleviate all voltage difficulties on the two feeders 1,2. One DC-link capacitor (CDC) powers these three VSI structures, which are coupled to a multi-feeder distribution system via 1:1 transformers. The suggested MDsUPQC topology may improve PQ and the sharing of load between neighboring feeders in a multi-feeder system. Without a requirement for extra power, the MDsUPQC minimizes all types of interruptions in feeder-1. The second side of the line transformers (LT-1 and LT-3) is linked in series to the main feeder-1 and neighboring feeder-2.

In this configuration, the MDsUPQC shunt VSI-2 in feeder-2 minimizes all current-related problems including current harmonic imperfections, load balancing, reactive power management, and power-factor adjustment caused by power-electronic non-linear load and maintains the voltage at the DC link as constant. The series VSIs-1,3 of MDsUPQC in both feeder-1 and feeder-2 alleviate all voltage-related concerns such as harmonics that are voltage distractions, imbalance voltage, sag in voltage, and voltage swelling, and 38% of the power available from a feeder-2 has been injected. In this configuration, feeder-2 is connected to a very sensitive non-linear (NL-2) load composed of three-phase uncontrolled-rectifier (UBR) loads that supply converting energy to a resistive-inductive RL-load together. The suggested MDsUPQC topology is shown schematically in Figure 1.

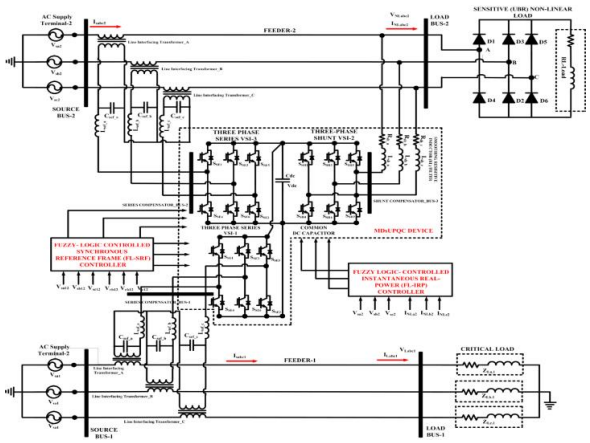


Figure 1. Schematic diagram of MDsUPQC topology for PQ enhancement

3. CONTROL STRATEGIES

3.1. Proposed fuzzy-logic controlled synchronous reference frame control scheme for series VSIs-1,3 of MDsUPQC topology

In general, the MDsUPQC series VSI-1,3 functions as voltage-controlled devices of a multi-feeder distribution network to regulate the common-coupling voltage with regard to the basic value of the load voltage. Using Park's transformation technique, the measured actual supply voltages (V_{sabc1} and V_{sabc2}) in a standard ABC-frame are transferred into direct (d-axis) and quadrature (q-axis) axes ($V_{sdq0.12}$) in a rotating reference frame. The measured dq supply terminal voltage ($V_{sdq0.12}$) is approximated with the dq reference voltage (V_{rabc12}) after the dq transformation process to obtain the perfect compensated reference voltage with error sequences. These error sequences are minimized using the trail-error approach and a PI controller with proper proportional gain (Kp.r) and integral gain (Ki.r) choices. The transfer function of the voltage controller is as (1).

$$V_{err}(s) = \left(k_{p.s} + \frac{k_{i.s}}{s}\right) \times E_{err}(s) \quad (1)$$

The performance of a PI controller is always dependent on the selection of feasible gains with necessary steps using the Ziegler-Nichols method. Because of this method, the traditional PI controller does not auto-tune the gain values during parametric variations, sudden variations, and affecting the overall system stability. It is realized the importance of an intelligent FL controller in the symbolic characterization of an inference system with considerable expert knowledge. This FL controller exemplifies the intelligent knowledge-based process, which includes FL-membership functions and an FL-rule base [11], [15]–[19]. The FL-rule base is the heart of FL control and the gathering of necessary information for depicting data manipulation values, linguistic models, and FL-rule characterization, among other things.

$$V_{err}(s) = V^*_{rdq0.12} - V_{sdq0.12} \quad (2)$$

$$\Delta V_{err}(s) = V_{err}(s) - V_{err}(s-1) \quad (3)$$

Where, $V_{err}(s)$ and $\Delta V_{err}(s)$ are the error and change in error. The related FL-membership functions and FL-rule base are shown in Figure 2 and Table 1.

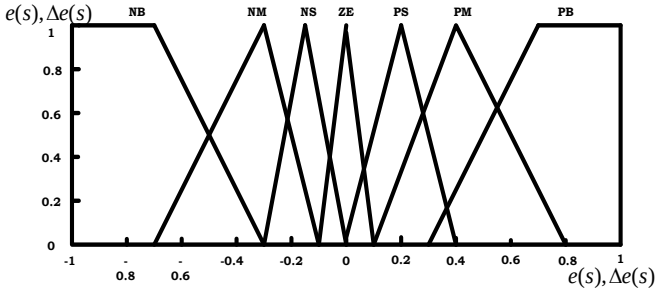


Figure 2. FL membership functions

Table 1. FL-rule-base

$e(s), \Delta e(s)$	NB	NM	NS	ZE	PS	PM	PB
NB	NB	NB	NB	NB	NM	NS	ZE
NM	NB	NB	NB	NM	NS	ZE	PS
NS	NB	NB	NM	NS	ZE	PS	PM
ZE	NB	NM	NS	ZE	PS	PM	PB
PS	NM	NS	ZE	PS	PM	PB	PB
PM	NS	ZE	PS	PM	PB	PB	PB
PB	ZE	NM	NS	ZE	PS	PM	PB

Therefore, error sequences are reduced in the FL-SRF controller, which generates the appropriate reference voltage signals in the dq-frame ($V^*_{refdq.12}$) as in (4). Then, using the inverse-Park's transformation the procedure stated in (5), these voltages are retransformed into the ABC standard frame.

$$V^*_{refdq.12} = (V_{rdq0.12} - V_{sdq0.12}) \tag{4}$$

$$\begin{bmatrix} V^*_{refa.12} \\ V^*_{refb.12} \\ V^*_{refc.12} \end{bmatrix} = \frac{2}{3}\begin{bmatrix} cos\theta & sin\theta & 1 \\ cos\left[\theta - \frac{2\pi}{3}\right] & sin\left[\theta - \frac{2\pi}{3}\right] & 1 \\ cos\left[\theta + \frac{2\pi}{3}\right] & sin\left[\theta + \frac{2\pi}{3}\right] & 1 \end{bmatrix}\begin{bmatrix} V^*_{refd.12} \\ V^*_{refq.12} \end{bmatrix} \tag{5}$$

The generated reference voltage signals ($V^*_{refabc.12}$) are transferred to the sinusoidal pulse width modulation (PWM) approach for the production of possible switching pulses to the series connected VSI-1,3 of the MDsUPQC topology, which eliminates all voltage-related PQ problems. The schematic diagram of the proposed FL-controlled FL-SRF control scheme for series VSI-1,3 of MDsUPQC topology is shown in Figure 3.

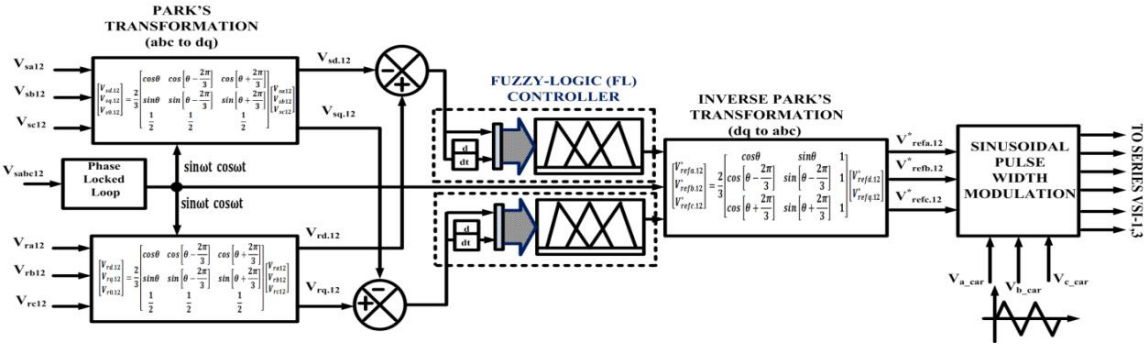


Figure 3. Schematic diagram of proposed FL controlled FL-SRF control scheme for series VSI-1,3 of MDsUPQC topology

3.2. Proposed fuzzy-logic controlled IRP controller for shunt VSI-2 of MDsUPQC topology

In general, the MDsUPQC shunt VSI-2 functions as a current-controlled apparatus at a multi-feeder distribution system's point of common coupling (PCC) to handle current-related PQ concerns [20]–[22]. The suggested FL-IRP control approach typically uses Clarke's conversion technique to convert conventional ABC into *αβ* symmetric coordinates in a fixed reference frame. The instantaneous real and reactive power in a symmetrical coordinate frame is calculated using (10) and (11) as shown in (6) and (7).

$$p = v_{s\alpha 2} i_{NL\alpha 2} + v_{s\beta 2} i_{NL\beta 2} \tag{6}$$

$$q = -v_{s\beta 2} i_{NL\alpha 2} + v_{s\alpha 2} i_{NL\beta 2} \tag{7}$$

The non-linear distorted load currents in symmetrical αβ-frame are stated as (8).

$$\begin{bmatrix} i_{NL\alpha 2} \\ i_{NL\beta 2} \end{bmatrix} = \frac{1}{\Delta_k}\begin{bmatrix} v_{s\alpha 2} & v_{s\beta 2} \\ -v_{s\beta 2} & v_{s\alpha} 2 \end{bmatrix}\begin{bmatrix} p \\ q \end{bmatrix} \tag{8}$$

Where,

$$\Delta_k = v^2_{s\alpha 2} + v^2_{s\beta 2} \tag{9}$$

The resulting actual currents are then routed via a second-order high-pass filter, allowing more advanced elements to get particular signals that act as references. The high-frequency sections are treated, resulting in a component loss denoted as (P.Loss). In addition, the suggested FL control in the DC control section, which is coupled to the primary controller, keeps the DC voltage of the shunt-connected VSI-2 stable. This FL controller exemplifies the intelligent knowledge-based process, which includes FL membership functions and an FL-rule base. These FL-membership functions and FL-rules are key components in FL controllers by incorporating significant human knowledge into an artificial knowledge base. The DC control section corrects errors induced by the variation of the real DC voltage ($V_{dc.c}$) and the

corresponding reference DC voltage ($V^*_{dc.r}$). The (10) and (11) show the outcome of the controlling component at the nth point.

$$V_{dc.cer} = V^*_{dc.r} - V_{dc.c} \tag{10}$$

$$\Delta_{ia.dc} = K_{p.d} * \left(V_{dc.cer(n)} - V_{dc.cer(n-1)}\right) + K_{i.d} * \left(V_{dc.cer(n)}\right) \tag{11}$$

The FL controller has a highly robust performance, is model-free, has a high strength index, and is operated as a subjective decision based on a universe-approximation technique with an FL rule-based algorithm. The related FL-membership functions and FL-rule base are depicted in Figure 2 and Table 1. These immediate elements can be expressed as DC oscillating and AC averaging values, respectively.

$$\begin{aligned} p &= \bar{p} + \tilde{p} \\ q &= \bar{q} + \tilde{q} \end{aligned} \tag{12}$$

Where, $\tilde{p}\tilde{q}$ denotes oscillated AC values, $\bar{p}\bar{q}$ denotes the averaged DC values. In addition, the extracted reference current signal ($i^*_{cr.\alpha\beta}$) in αβ symmetrical frame is described as (13).

$$\begin{bmatrix} i^*_{cr.\alpha 2} \\ i^*_{cr.\beta 2} \end{bmatrix} = \frac{1}{\Delta_k} \begin{bmatrix} v_{st.\alpha 2} & -v_{st.\beta} 2 \\ v_{st.\beta 2} & v_{st.\alpha 2} \end{bmatrix} \begin{bmatrix} p \\ q \end{bmatrix} \tag{13}$$

Figure 4 depicts a schematic representation of the planned FL-IRP control method for MDsUPQC's shunt VSI-2. As a consequence, the acquired currents of reference ($i^*_{cr.\alpha\beta 2}$) in the $\alpha\beta$-frame are reverted into the basic ABC frame using the inverse Clarke's translation process, yielding the ultimate reference current ($i^*_{cr.abc2}$) as given in (14):

$$\begin{bmatrix} i^*_{cr.a2} \\ i^*_{cr.b2} \\ i^*_{cr.c2} \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1/\sqrt{2} & 1 & 0 \\ 1/\sqrt{2} & -1/2 & \sqrt{3}/2 \\ 1/\sqrt{2} & -1/2 & -\sqrt{3}/2 \end{bmatrix} \begin{bmatrix} i^*_{c.02} \\ i^*_{c.\alpha 2} \\ i^*_{c.\beta 2} \end{bmatrix} \tag{14}$$

Finally, the reference currents extracted from the proposed FL-IRP control scheme are contrasted with the actual supply currents for the production of switching pulses to the VSI-2 of the MDsUPQC device via hysteresis current-control (HCC) as gate-pulse generation unit. The HCC is utilized for the production of possible switching states to VSI-2 of the MDsUPQC through HCC band limits, which are regarded as limit values of compensation currents that are rotated across the upper/lower limits of HCC bands. The schematic diagram of the proposed FL-IRP control scheme for shunt VSI-2 of MDsUPQC topology is shown in Figure 4.

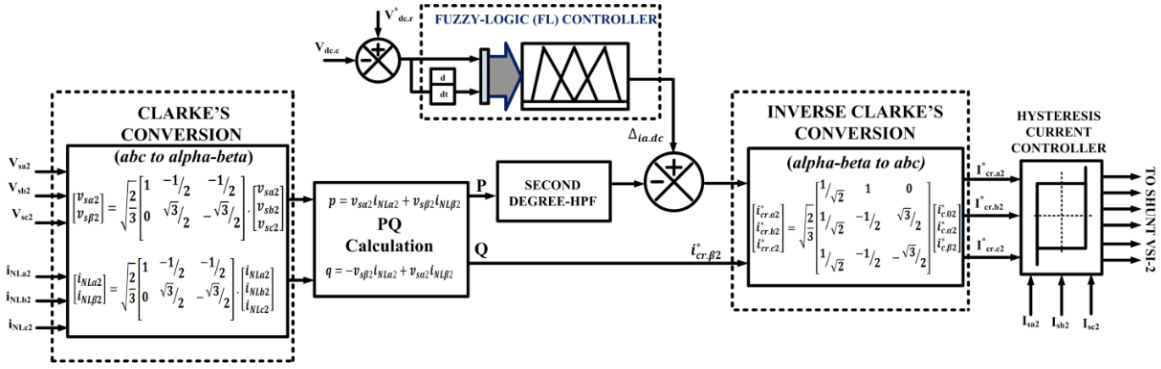


Figure 4. Schematic diagram of proposed FL-IRP control scheme for shunt VSI-2 of MDsUPQC topology

4. RESULTS AND DISCUSSION

The performance of the suggested FL-controlled MDsUPQC device for PQ improvement, load sharing across feeders, and simulation results are shown with an appealing comparison analysis. Table 2 shows the operational parameters and values of the proposed MDsUPQC topology as generalized estimated values from many literature researches.

Table 2. Operating parameters and values of proposed MDsUPQC topology

S. No	Parameters	Values	
		Feeder-1	Feeder-2
1	Three-phase source voltage (V_{rms})	V_{sabc12}-415 V, 50 Hz	
2	Line impedance	R_{s12}=0.15 Ω, L_{s12}-0.9 mH	
3	Critical and sensitive load impedances	R_L=30 Ω, L_L-20 mH (NL-load)	V_L=415 V, 50 Hz, P_L=10 KW, Q_L=5 KVar (critical load)
4	Linear (1:1) transformer	415 V, 50 Hz, linear model-5 KVA, 10% leakage reactance	
5	Series-connected VSIs-1,3 filters	L_{se}-3 mH, C_{se}-100 µF	
6	Shunt-connected VSI-2 filters	--	R_{sh}= 0.001 Ω, L_{sh}-10 mH
7	Common DC-link capacitor	$V_{dc.c}$= 880 V, $C_{dc.c}$ =1500 µF	

4.1. Performance evaluation of series-connected VSI-1 of MDsUPQC in feeder-1 using proposed fuzzy-logic controlled SRF control scheme

Simulation outcomes of series VSI-1 of FL-SRF-driven MDsUPQC in feeder-1 under voltage harmonics are displayed in Figure 5. This feeder-1 is supplied with a voltage of 415 Vrms, 50 Hz supply system to accomplish the critical load system. Regarding voltage harmonics, during 0.85 sec and 0.95 sec, the main voltage is impacted by 5th and 7th-order harmonics, which present a major issue in feed-1. At this period, the FL-SRF-driven MDsUPQC's series VSI-1 injects the necessary voltage using the in-phase opposing concept to minimize voltage harmonics in the load voltage while offering a harmonic-free response. Figure 6 depicts harmonic analysis. Total harmonic distortion (THD) analysis of the source voltage reaches 20.62% while harmonic presence is shown in Figure 6(a) and 0.43% while harmonic removal as shown in Figure 6(b), which is substantially within IEEE-519/2014 requirements adjusted by series VSI-1 of FL-SRF controlled MDsUPQC.

The effectiveness of the FL-SRF controlled MDsUPQC series VSI-1 in feeder-1 is validated under voltage-sag, as illustrated in Figure 7. Because voltage sag does not exist in feeder-1, the source voltage remains constant at 340 V while in the pre-sag state. When voltage sag is introduced in feeder-1 within 0.1 and 0.2 sec, the source voltage decreases slightly to 170 V because of sag in the source. The load voltage remains constant at 340 V, however, since the series VSI-1 of feeder-1 introduces the needed voltage of 170 V to maintain the load voltage as stable. As shown in Figure 8, the functioning of the series VSI-1 of the FL-SRF-driven MDsUPQC in feeder-1 is validated under voltage swell.

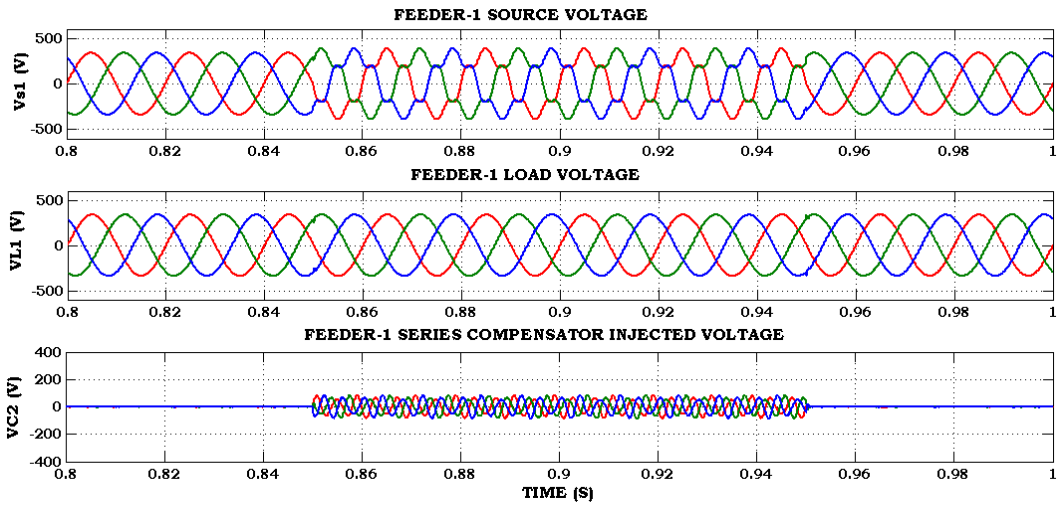
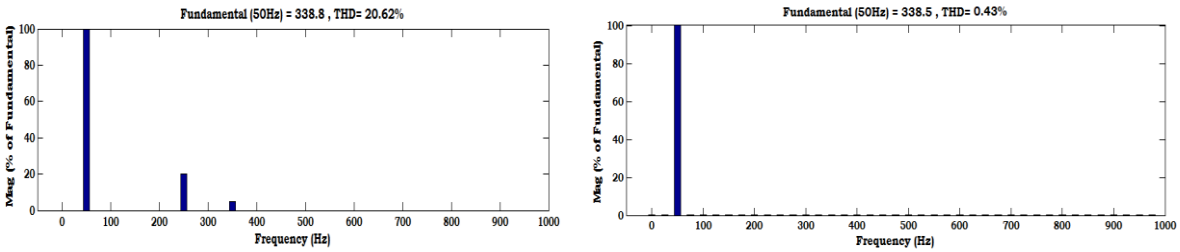


Figure 5. Simulated results of series-connected VSI-1 of FL-SRF controlled MDsUPQC in feeder-1 under voltage harmonics



(a) (b)

Figure 6. THD spectrum in feeder-1 during voltage harmonics of (a) source and (b) load voltage values

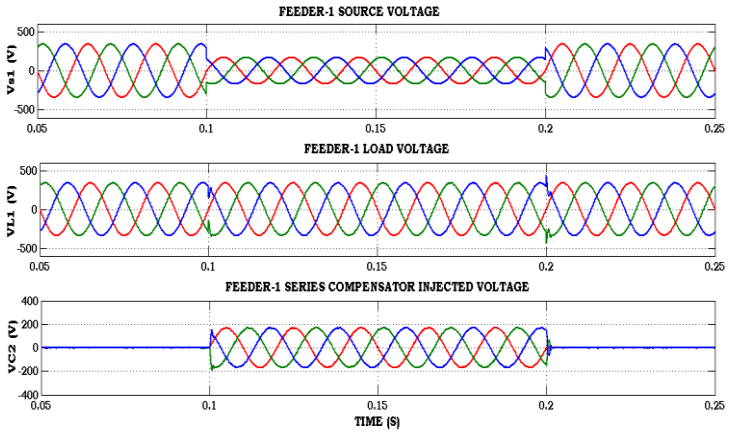


Figure 7. Voltage sag condition

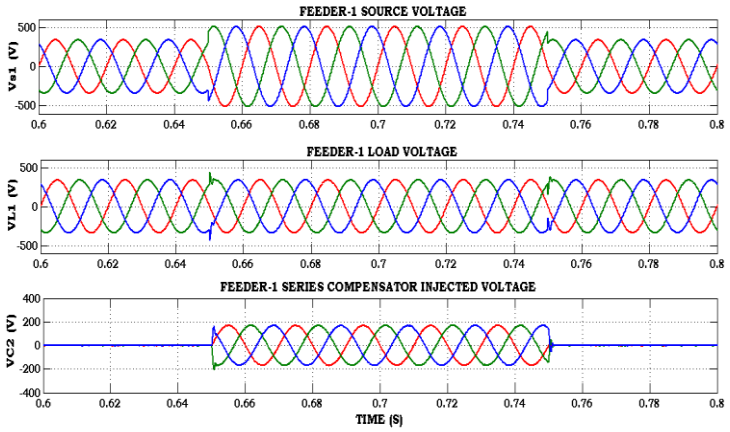


Figure 8. Voltage swell condition

Because voltage swelling does not occur in feeder-1, the source's voltage remains stable at 340 V while in the pre-swell state. Voltage swelling happens during 0.65 sec and 0.75 sec in feeder-1 due to swell in the source voltage rising to 510 V. The load voltage remains stable at 340 V since the series VSI-1 of feeder-1 injects/absorbs the extra voltage of 170 V to maintain the voltage of the load as constant. Under voltage interruptions, the capability of the series-linked VSI-1 of the FL-SRF-driven MDsUPQC in Feeder-1 is validated, as illustrated in Figure 9. Because these don't exist voltage disruptions in feeder-1, the source's voltage is maintained stable at 340 V until 0.35 sec. While voltage disruptions occur in feeder-1 within 0.35 and 0.55 sec, the source voltage decreases to 0 V, affecting the load voltage while the compensator is not enabled. The load voltage, however, remains stable at 340 V since the series VSI-1 of feeder-1 injects the needed voltage of 430 V to maintain the voltage of the load as stable.

Figure 10 shows the active reactive power of the source, load, and series connected VSI-1 of MDsUPQC topology in Feeder-1. The active power of the primary source remains consistent at 10 KW while in the pre-sag state prior to 0.1 sec; while the voltage sag is given during 0.1 sec and 0.2 sec in feeder-1, the source's active power is somewhat lowered to 5 KW owing to the rapid voltage-sag situation. In such an instance, the series VSI-1 of the MDsUPQC introduces the required active power to the load, which is kept steady at 5 KW in order to maintain the load's active power as constant at 10 KW, as shown in Figure 10(a).

In addition, while in the pre-sag state, the reactive power of the source remains consistent at 5 KVar. The reactive power of the source is lowered to 2.5 KVar under the sagging state; the series linked VSI-1 of the MDsUPQC introduces the required reactive power of 2.5 KVar to the load, which keeps the load's reactive power as stable at 5 KVar, as illustrated in Figure 10(b). In a similar way for each of the prior situations, the active and reactive powers are maintained as constant by employing the series VSI-1 of MDsUPQC to improve the PQ characteristics in the feeder-1 of the multi-feeder distribution network.

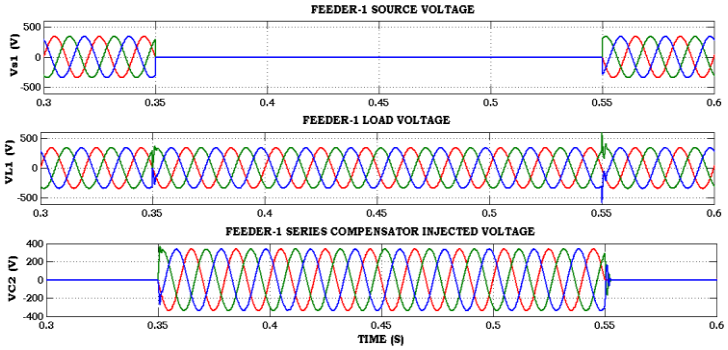
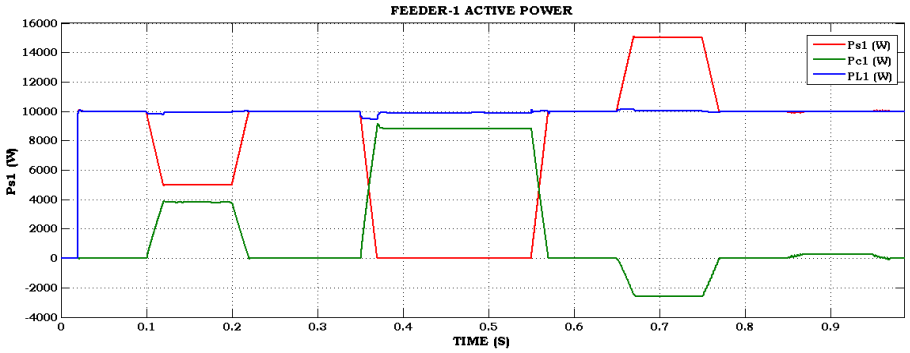
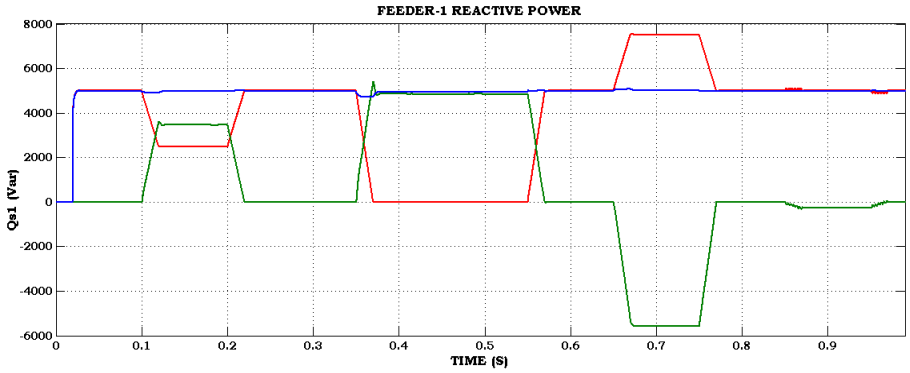


Figure 9. Simulated results of series-connected VSI-1 of FL-SRF controlled MDsUPQC in feeder-1 under voltage interruptions condition



(a)



(b)

Figure 10. Series connected source, load, VSI-1 of MDsUPQC topology in feeder-1 of (a) active power and (b) reactive power

4.2. Performance evaluation of series-connected VSI-3 and shunt VSI-2 of MDsUPQC in feeder-2 using proposed fuzzy-logic controlled SRF/IRP control scheme

Figure 11 depicts the simulated results of the shunt VSI-2 of the MDsUPQC in feeder-2 under current harmonic distortions. With a 415 V, 50 Hz supply system, feeder-2 has been energizing the three-phase non-linear UBR load. The source current is distorted and harmonized as a result of these non-linear power loads, producing serious issues in feeder-2 and increasing heat loss; the flow of extremely high rates destroys the whole load system. To eliminate harmonics from the NL-UBR load, a shunt-connected VSI-2 of MDsUPQC has been employed in the FL-IRP control scheme. As an in-phase opposition principle, the proposed MDsUPQC of shunt-connected VSI mitigates all harmonic distortions and furnishes the pure-sinusoidal voltage, and current with balanced nature.

The THD spectrum of source and load current values in feeder-2 in the presence of harmonic current distortions is depicted in Figure 12. THD of non-linear power load current due to non-linear load switching is nearly 30.05% (Figure 12(a)), and harmonic distortions in the supply current have been eliminated with an average of 2.71% (Figure 12(b)), both of which falls well in IEEE-519/2014 standards provided by FL-IRP controlled by shunt VSI-2 of MDsUPQC architecture. The DC-link capacitor voltage remains constant at 880 V with the help of the recommended FL controller, which maintains the PCC voltage stable as depicted in Figure 13. As shown in Figure 14, the supply current is in phase with the voltage of the supply and defines the identical power factor at the point of connection of feeder-2 in a multi-feeder distribution network.

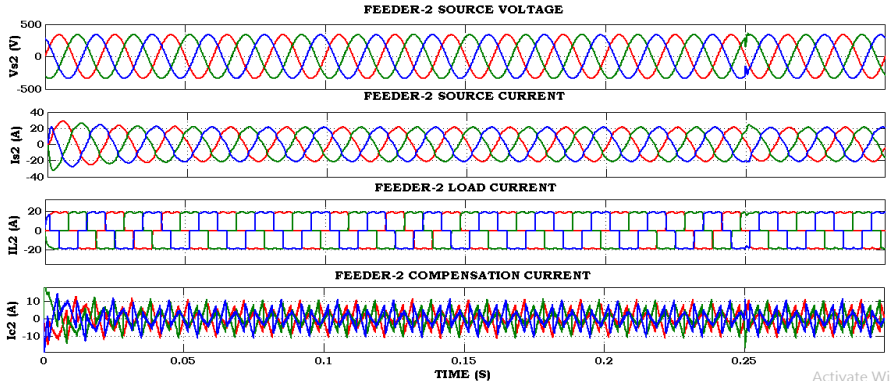


Figure 11. Simulated results of shunt-connected VSI-2 of FL-IRP controlled MDsUPQC in feeder-2 under non-linear load

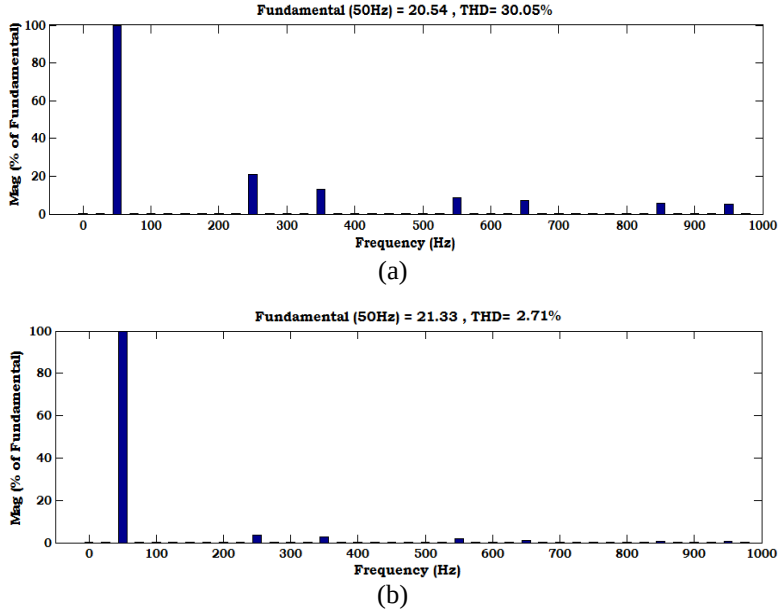


Figure 12. THD spectrum of feeder-2 during the presence of harmonic current distortions on (a) non-linear load current and (b) supply current

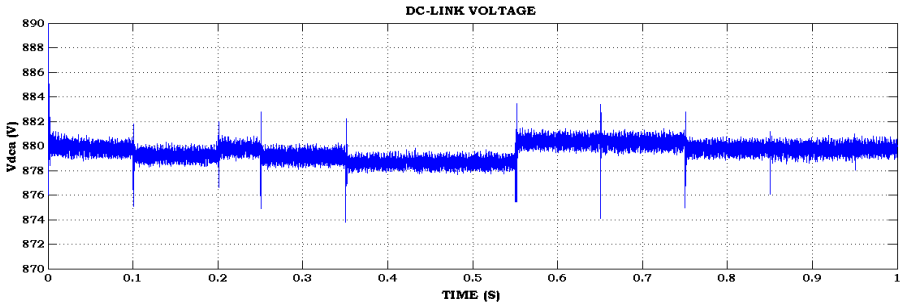


Figure 13. DC-link voltage

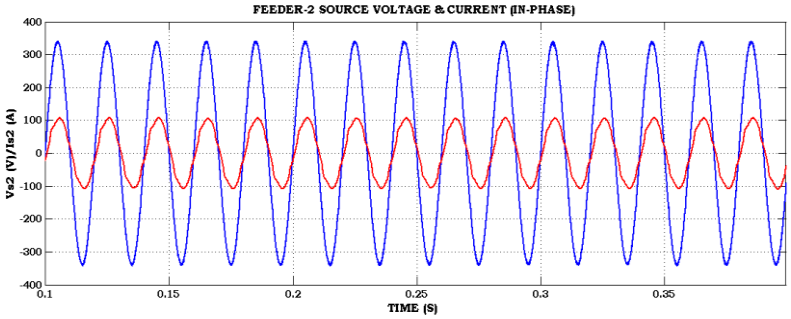


Figure 14. Supply voltage and supply current

Figure 15 depicts the simulated results of a series VSI-3 of FL-SRF-operated MDsUPQC in feeder-2 during voltage sag conditions. While voltage sag does not exist in feeder-2, the source voltage is held stable at 340 V throughout the pre-sag condition. Due to the existence of voltage sag in the main input supply, the voltage of the supply is lowered to 50% of the base value in feeder-2 during 0.25 sec and 0.35 sec. The load voltage, even so, remains stable at 340 V due to the series VSI-3 of feeder-2 introducing the required voltage of 170 V to maintain the essential load voltage as constant. The operation of the series VSI-3 of the MDsUPQC in feeder-2 is demonstrated in Figure 16 under voltage-swell circumstances. Because voltage swell does not occur in feeder-2, the source voltage remains constant at 340 V throughout the pre-swell condition. Table 3 and Figure 17 depict the time instant between 0.55 sec supply voltage and critical load voltage in feeder-2 of a multi-feeder distribution system. Table 4 and Figure 18 show the distribution system at the time instant between 0.55 sec. Because voltage swell does not occur in feeder-2, the source voltage remains constant at 340 V throughout the pre-swell condition. Table 4 and Figure 18 provide THD comparisons and a graphical view of non-linear load current and supply current in feeder-1 of a multi-feeder distribution system.

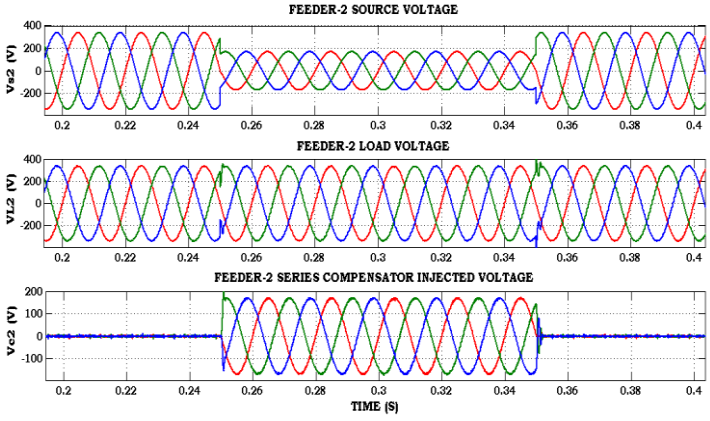


Figure 15. Voltage sag condition

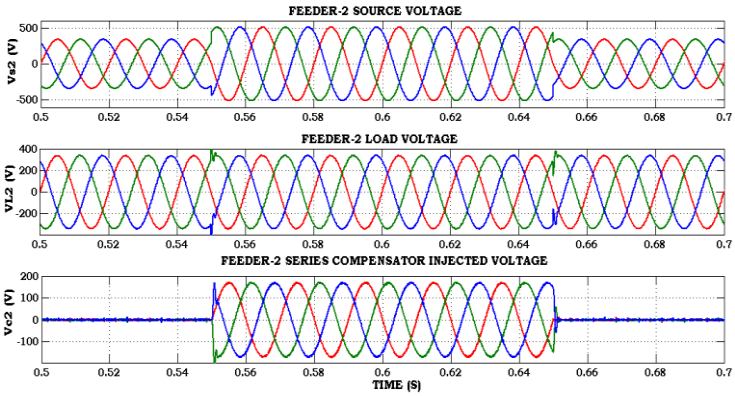


Figure 16. Voltage swell condition

Table 3. THD comparisons of supply voltage and critical load voltage in feeder-2 of multi-feeder distribution system

THD	Supply voltage (%)	Critical load voltage (%)
Without MDsUPQC topology	20.68	20.68
With PI-SRF-controlled MDsUPQC topology [13]	20.62	0.52
With the proposed FL-SRF controlled MDsUPQC topology	20.62	0.43

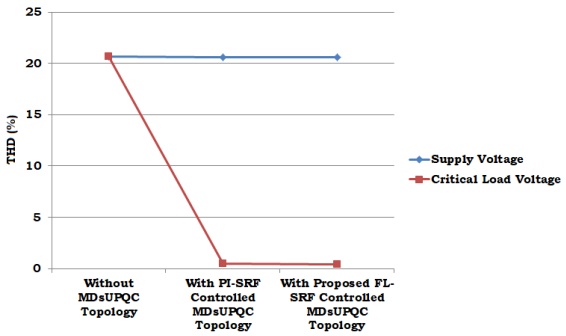


Figure 17. Graphical view of THD comparisons in feeder-2 of the multi-feeder distribution system

Table 4. THD comparisons of non-linear load current, supply current in feeder-1 of multi-feeder distribution system

THD	Non-linear load current (%)	Supply current (%)
Without MDsUPQC topology	30.07	30.07
With PI-IRP controlled MDsUPQC topology [14]	30.05	5.20
With the proposed FL-IRP controlled MDsUPQC topology	30.05	2.71

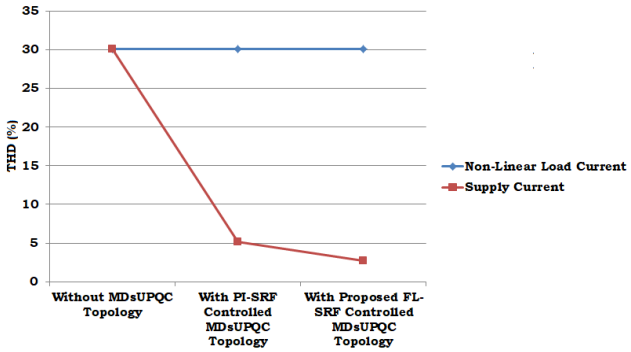


Figure 18. Graphical view of THD comparisons in feeder-1 of the multi-feeder distribution system

5. CONCLUSION

The suggested FL-controlled MDsUPQC topology for PQ improvement in a multi-feeder distribution system was critically evaluated. By combining considerable human knowledge into an artificial knowledge base, this FL controller exhibits an intelligent knowledge-based process. Over traditional control systems, the suggested FL controller SRF/IRP-driven MDsUPQC architecture mitigates all voltage-current allied PQ concerns. The performance of the suggested FL-controlled MDsUPQC device for PQ improvement, load sharing across feeders, and simulation results are shown with an appealing comparison analysis. THD analysis of source voltage reaches 20.62% during harmonic presence and 0.43% during harmonic removal, which is well within IEEE-519/2014 requirements adjusted by series connected VSI-1 of FL-SRF controlledMDsUPQC. THD spectrum of source and load current values in feeder-2 in the presence of harmonic current distortions. The THD of non-linear current at the load is almost 30.05%, and harmonic distortions in supply current are eliminated with a value of 2.71%, both of which are well within IEEE-519/2014 norms compensated by FL-IRP controlled by shunt-connected VSI-2 of MDsUPQC topology.

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