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A novel reduced-switch multi-level inverter based multi-device universal power-quality conditioner for PQ enhancement

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ABSTRACT

The reduced-switch multilevel inverter (RSMLI) has garnered significant attention across various industries as a viable alternative to conventional multilevel inverter (MLI) topologies. In the realm of medium voltage high-power applications, the topologies of resonant switched MLIs are regarded as advanced due to their development with a reduced number of switching elements. The primary emphasis of the customizable multi-device universal power-quality conditioner (MD-UPQC) device is on the design and development of a significant RSMLI topology to improve power-quality (PQ) features. This study presents the development of a novel 5-level RSMLI-based MD-UPQC device, designed specifically for addressing power-quality concerns in multi-feeder distribution networks. The device facilitates uninterrupted power flow between the feeders, thereby mitigating power-quality issues. The 5-level RSMLI topology possesses the capability to decrease the necessity for a larger quantity of gate-drive circuits by implementing a switching-logic design utilizing the reduced-carrier-based pulse width modulation (PWM) technique. The 5-level RSMLI-MDUPQC device incorporates a unified voltage-current reference (UVCR) control scheme to ensure efficient operation. The functionality and efficacy of the proposed RSMLI-MDUPQC device have been assessed using the MATLAB/Simulink software tool, with the evaluation conducted under different PQ conditions. The simulation outcomes are presented for analysis and interpretation.

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1. INTRODUCTION

The significance of power quality (PQ) in multi-feeder electrical distribution networks is widely acknowledged due to its profound effects on both utility systems and end-level customers [1]. The proliferation of PQ deviations and distortions can be attributed to the utilization of large-sized switch-mode power converters, arc furnaces, variable speed motors, and the switching of massive non-linear loads in the secondary distribution level [2]. The issue at hand pertains to the PQ of the network, specifically regarding the frequency, current, and terminal voltage. These parameters exhibit non-sinusoidal characteristics and include harmonized components. The primary causes and origins of current quality issues include the generation of harmonic current distortions, reduction in reactive power, non-unity power factor, and unbalanced loads. The presence and origins of voltage quality issues give rise to harmonic voltage

distortions, voltage deviations, voltage sags and swells, and unbalanced voltage. These phenomena indicate the presence of contaminated power at the common-feeding point of a multi-feeder network [3].

In this context, numerous power-system engineers are compelled to develop contemporary PQ enhancement devices through the utilization of customized power (CP) compensation technology. The utilization of custom-power devices in this CP technology serves to address voltage and current PQ issues, resulting in the establishment of a multi-feeder network that exhibits sinusoidal, linear, fundamental, and balanced characteristics [4]. The categorization of multi-feeder customized compensation devices is based on specific PQ effects and concerns, including interline power flow controller (I-PFC) [5], interline dynamic voltage restorer (I-DVR) [6], and interline unified power-quality conditioner (I-UPQC) [7]. Among the devices discussed above, the multi-device universal power-quality compensator (MD-UPQC) was created particularly for multi-feeder distribution networks [8]. The system may send and receive active and reactive power between feeders, efficiently correcting for voltage and current-related PQ issues. This guarantees that high-quality electricity is available in a multi-feeder distribution network.

The MD-UPQC device's setup is described in reference [9], where it is greatly improved by utilizing multiple 3-level voltage-source inverters (VSIs) coupled in a back-to-back arrangement. Using a common DC-link source, the numerous three-level VSIs are set in a shunt-shunt, shunt-series, and series-shunt configuration between the multi-feeders. The study describes a novel multi-converter unified power-quality conditioner (MC-UPQC) designed to enhance PQ attributes in a multi-feeder distribution system. This is accomplished by combining many VSI modules. The details of this UPQC are discussed in reference [10]. The primary concerns associated with conventional three-level VSI compensation devices have been investigated in previous studies [8]–[10]. These devices are subject to several limitations, including elevated rates of change of voltage (dv/dt) and current (di/dt), generation of square-wave output voltage, requirement for substantial load side filtering, presence of high common-mode voltage, necessity for large peak-current ratings, high initial costs, limited reverse-voltage blocking capacity of switches, and increased electromagnetic losses, among others. To address the aforementioned constraints in three-level VSIs, it is suggested that the implementation of multi-level inverters (MLIs) topologies be considered for medium voltage and high-power compensation devices [11]. In general, MLIs generate Alternating current (AC) output voltage that closely approximates a sinusoidal waveform by utilizing the switching of switches connected to input direct current (DC)sources or capacitors [12]. The diode-clamped multilevel inverter (DCMLI) [13], flying-capacitor multilevel inverter (FCMLI) [14], and cascade H-bridge multilevel (CHMLI) [15] topologies are among the different MLI topologies that have been developed.

The number of output voltage levels in MLI topology is directly correlated with the quantity of switching elements employed. As the number of levels increases, there will be a corresponding increase in the quantity of switching elements. Conventional topologies are not well-suited for higher voltage levels due to their increased cost, the requirement for additional switching devices, complex gate-drive circuitry, and the need for additional clamping diodes and storage capacitors. The advancement in MLI topologies has led to the development of novel reduced-switch multilevel inverters (RSMLIs). These inverters have been designed to require fewer switching devices, achieved through the implementation of symmetrical and asymmetrical switching arrangements.

Several RSMLI topologies have been developed by researchers and are presented in references [16]–[22]. The RSMLI topologies have garnered significant attention in the research community due to their ability to perform high-voltage medium-power operations. The primary aim of the proposed novel RSMLI topology is to generate high-quality AC staircase output while utilizing a reduced number of switches, low input DC sources, minimized gate-drive circuits, and mitigating issues such as low dv/dt stress, reduced efficiency, and electromagnetic loss. The primary objective of the proposed study is to introduce a novel 5-level RSMLI topology. This topology aims to address the voltage-current-related PQ issues in a multi-feeder distribution system by developing a novel RSMLI-UPQC device. Nevertheless, it possesses the capability to satisfy the improved PQ characteristics by effectively reducing harmonic distortions through the utilization of pulse width modulation (PWM) techniques [23]–[25]. The novel reduced-carrier-based pulse width modulation (RCB-PWM) control technique has been employed in the control of switching operations, incorporating notable reference signal extraction schemes, within the realm of various PWM techniques.

The investigation conducted in [26], [27] explores the synchronous reference frame (SRF) control and instantaneous real-power (IRP) control schemes [28], [29], which are widely recognized methods for extracting reference voltage-current in power systems. These methods are subject to limitations such as intricate transformations, intricate mathematical logic, and response latency. This study employs a novel unified voltage-current reference (UVCR) control scheme to extract reference signals for the RSMLI-MDUPQC device, enabling the generation of fundamental reference signals. The functionality and efficacy of the proposed RSMLI-MDUPQC device have been assessed under different PQ conditions using the MATLAB/Simulink software tool. The outcomes of the simulations are thoroughly presented and discussed.

2. PROPOSED 5-LEVEL REDUCED-SWITCH MULTILEVEL INVERTER TOPOLOGY

The schematic design of the proposed 5-level RSMLI topology is depicted in Figure 1. In distinct, the proposed 5-level RSMLI is significant over the regular MLI and various RSMLI topologies for PQ enhancement in a distribution network. The proposed RSMLI-MDUPQC needs three modules of 5-level RSMLI topologies integrated back-to-back through a common DC capacitor. RSMLI-3 is connected in series form to feeder-1; MLI-2 and MLI-1 are connected in series-shunt form to feeder-2 through linear 1:1-line connected transformer and filter units. The association of RSMLI in MD-UPQC devices is the best choice for obtaining improved PQ features over the regular MLI topologies and then accepted technically, and economically for any PQ compensation device. The equations for the proposed 5-level RSMLI topology requiring 'k' number of input DC sources are described as (1)-(3).

$$Number\ of\ switches\ (M_{.switch}) = (k+1) \tag{1}$$

$$Number\ of\ voltage\ levels\ (N_{.levels}) = \{(M_{.switch} + k) - 2\} \tag{2}$$

$$Number\ of\ carrier\ signals\ for\ gate - drive\ circuitry = (k-1) \tag{3}$$

For generation of 5-level output voltage, it requires four switches named $S_{1.1}$, $S_{2.1}$, $S_{3.1}$, and $S_{4.1}$, three input DC sources $V_{dc.1}$, and $V_{dc.2}$, $V_{dc.3}$ across $C_{dc.1}$, $C_{dc.2}$, and $C_{dc.3}$, respectively. The self-balancing of capacitor voltages $V_{dc.1}$, $V_{dc.2}$, and $V_{dc.3}$ is one of the acute features of the proposed 5-level RSMLI topology. The magnitude of three capacitors is maintained constant with equal to the common DC-link voltage of the MD-UPQC device. The voltages of input DC capacitors are used to transform the 5-level staircase AC output voltage by switching the respective switches in an RSMLI topology using appropriate switching action furnished by gate-drive circuitry. The staircase 5-level output voltage levels are V_{dca}, 2 V_{dca}, 0 V_{dca}, -V_{dca}, -2 V_{dca}, respectively. The switching pattern of the proposed 5-level RSMLI topology is depicted in Table 1. "N" represents the ON-switches and "F" represents the OFF-switches in the proposed 5-level RSMLI topology.

The suggested RSMLI-MDUPQC switching pattern is regulated by suitable reference current-voltage signals generated by the proposed UVCR control method. In comparison to existing phase extraction approaches, the proposed UVCR control system does not require power transformation methods and offers reference signals with a minimum time delay. It generates reference signals by detecting the load voltage value and generating unified vector values in a pre-synchronized angle (s) using a discrete phase-locked loop (DPLL). The authors present the mathematical modeling and design of the suggested UVCR control method in [27]. The measured values and the derived reference current-voltage signals from the UVCR control scheme are propagated using the RCB-PWM approach. It creates switching states that are appropriate for the proposed 5-level RSMLI architecture of the MD-UPQC device for PQ enhancement in a multi-feeder distribution network.

However, multi-carrier-based PWM (MCB-PWM) has been implemented, which efficiently minimizes distortions and decreases EMI loss. The schematic diagram of the suggested UVCR control scheme for the RSMLI-based MD-UPQC device is shown in Figure 2. Carrier-based PWM techniques are divided into two types: phase-shifted-based PWM (PSB-PWM) and level-shifted-based PWM (LSB-PWM). A PSB-PWM approach requires many synchronized phase-shifted multi-carriers with a zero-cross of reference voltage or current and each carrier. With synchronization of reference and multi-carrier method, multiple synchronized level-shifted multi-carriers are required in an LSB-PWM technique.

For higher voltage levels, these approaches are unsuitable because more carriers are required which increases the complexity of gate-drive circuitry. A new RCB-PWM technique has been established for the proposed RSMLI topology. The representation of the RCB-PWM technique is depicted in Figure 3. It is used to distribute power evenly over the MLIs to enhance the fundamental output voltage and minimize harmonic distortion. The RCB-PWM technique is employed using k-1 carriers for the generation of N number of voltage levels. Hence, only two triangular carrier signals with equal carrier frequency and magnitude are used and compared with the reference signal received from the UVCR control scheme for the generation of 5-level output voltage and gate pulses for switches generated according to Table 1. These have been developed by using logic gates as switching logic design is depicted in Figure 4. The overall schematic of the proposed RSMLI-MDUPQC device is depicted in Figure 5. The working and performance of the proposed UVCR-controlled RSMLI-MDUPQC device under various PQ signatures have been evaluated through the MATLAB/Simulink software tool and simulation results are illustrated. The system specifications and the values are stated in [27] and depicted in Table 2.

Table 1. Switching arrangement of 5-level DCMLI structure

Switching pattern	DCMLI voltage (V_O)	Switching arrangement			
		$S_{1.1}$	$S_{2.1}$	$S_{3.1}$	$S_{4.1}$
SP-1	V_{dca}	F	N	F	N
SP-1	2 V_{dca}	N	F	F	N
SP-1	0 V_{dca}	F	F	N	N
SP-1	-V_{dca}	N	F	N	F
SP-1	-2 V_{dca}	F	N	N	F

Table 2. Proposed system parameters and values

S. No	Specifications	Values	
		Feeder-2	Feeder-1
1	Source terminal voltage ($V_{st.rms}$)	V_{st1}- V_{st2}-415 Vrms, 50 Hz	
2	Load parameters	$V_{L.2}$=415 Vrms, 50 Hz, R_{L1}=30 Ω, L_{L1}-20 mH	$V_{L.1}$=415 Vrms $P_{Load.1}$=10 KW, $Q_{Load.1}$=5KVar
3	Feeder impedance	$R_{st.1}$=0.15 Ω, $L_{st.1}$-0.9 mH	
4	1:1 line connected transformer (linear type)	V_t-415 V, P_t-5 KVA, X_t-10% of leakage reactance	
5	Carrier frequency	F_c-3050 Hz, MI_c-0 to1	
6	Series-RSMLI line connected filter	$L_{se.12}$- 3 mH, $C_{se.12}$-100 µF	
7	Shunt-RSMLI line connected filter	$R_{sh.2}$=0.001 Ω, $L_{sh.2}$-10 mH	
8	Common DC capacitor	$C_{dc.L}$=1500 µF, $V_{dc.L}$=880 V	

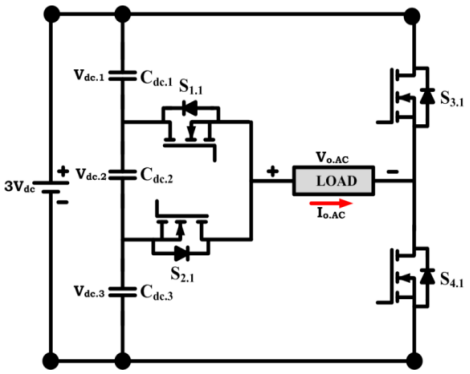


Figure 1. Schematic design of proposed 5-level RSMLI topology

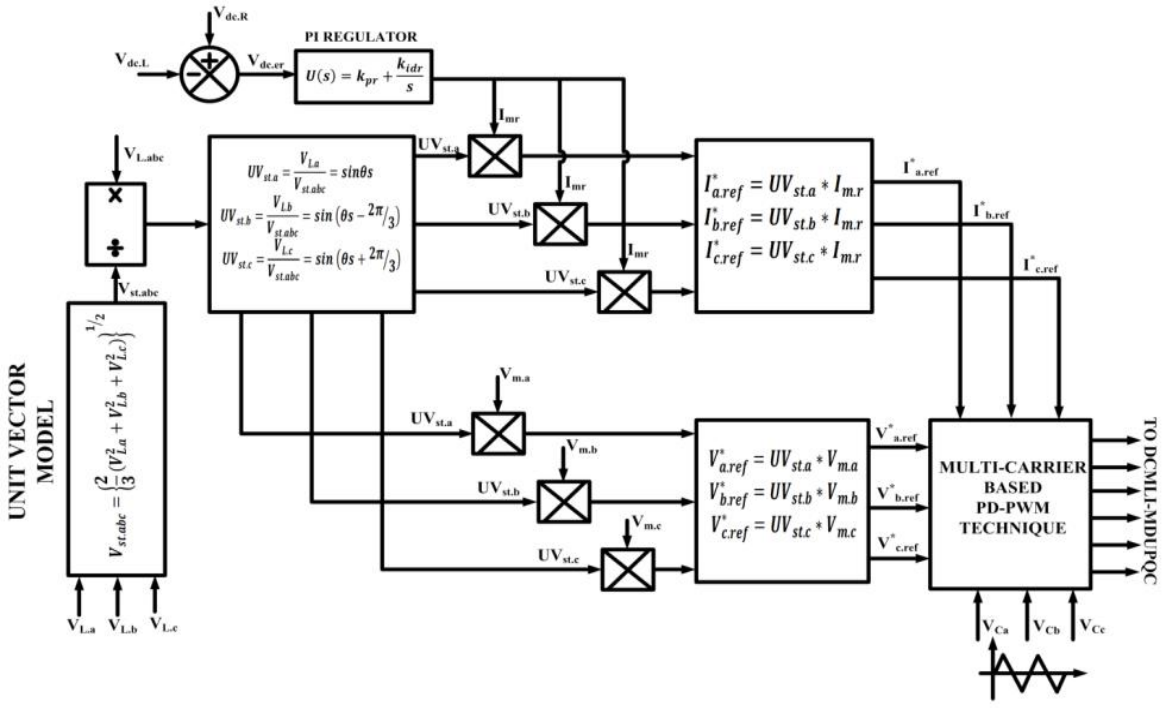


Figure 2. Schematic diagram of proposed UVCR control scheme for RSMLI-based MD-UPQC device

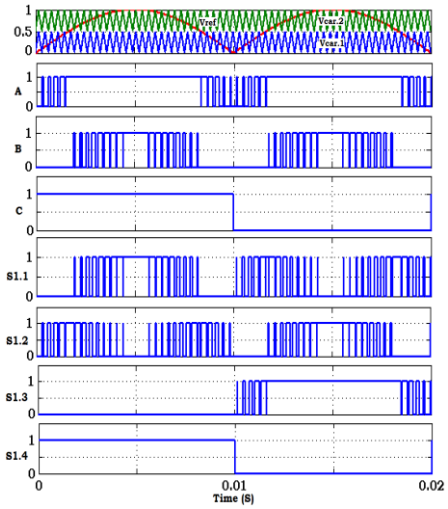


Figure 3. Representation of the proposed RCB-PWM technique

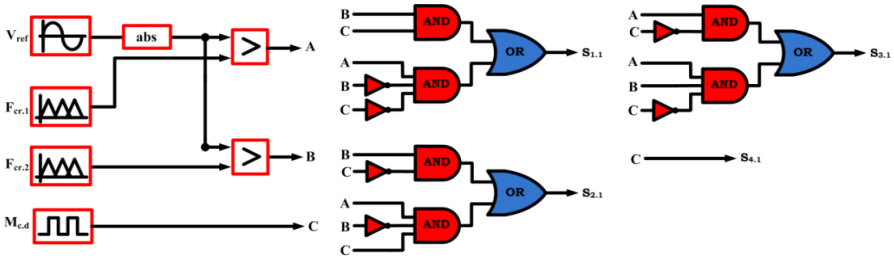


Figure 4. Switching logic design of proposed RCB-PWM technique

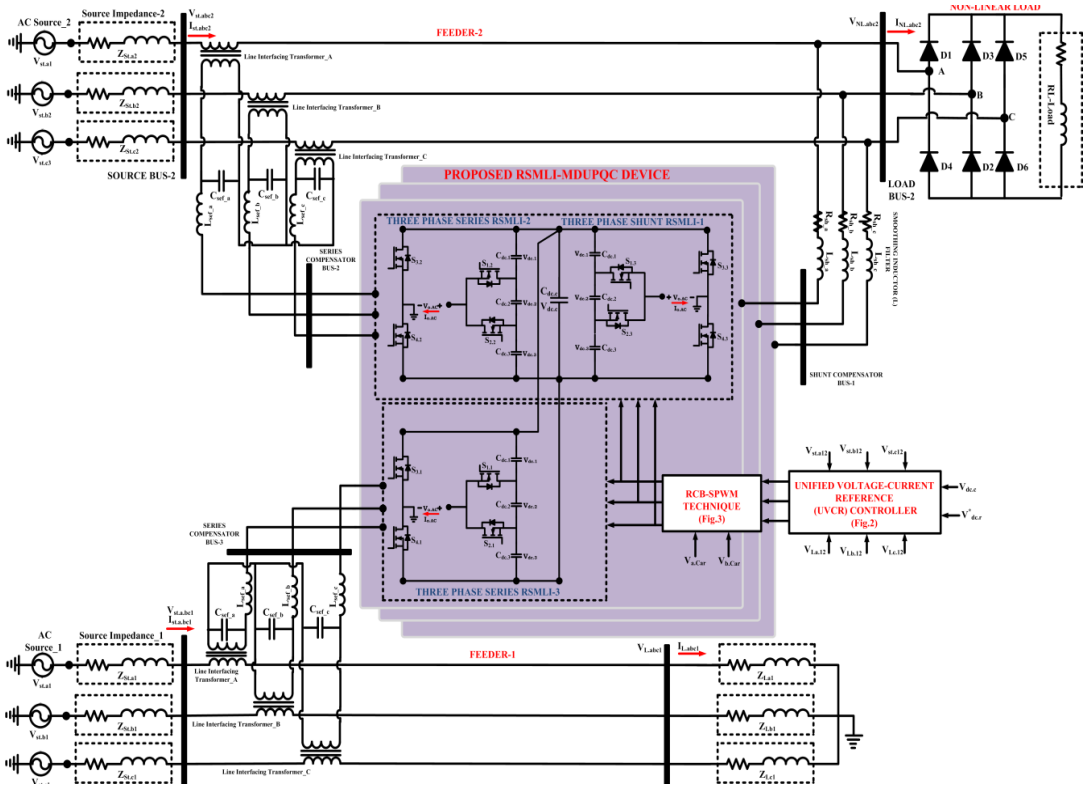


Figure 5. Overall schematic model of the proposed RSMLI-MDUPQC device

3. RESULTS AND DISCUSSION

3.1. Performance of UVCR-controlled proposed 5-level RSMLI-MDUPQC device for mitigation of current/voltage allied PQ issues in feeder-2

The simulation results of UVCR controlled suggested 5-level shunt RSMLI-1 of MD-UPQC device in feeder-2 for harmonic current correction is shown in Figure 6 (in Appendix). The two-feeder distribution network depicted in Figure 5 is designed for non-linear and critical loads using a three-phase 415 V, 50 Hz supply. The massive non-linear rectifier produces uneven harmonics in the source current affecting the smooth operation of other loads interfaced at the per-connection classifier (PCC) or end-user level. These harmonic distortions in source current are compensated by using 5-level RSMLI-1 of MD-UPQC device functioning in in-phase compensation mode. However, it enhances the reactive power, and power factor to make system parameters balanced, sinusoidal, linear, and fundamental nature in feeder-2 as shown in Figures 6(a)-(d). It adjusts the phase angle of the source current such that it is in phase with the source terminal voltage, as shown in Figure 6(e). According to IEEE-519/1992 standards, the total harmonic distortion (THD) value of non-linear load current in feeder-2 is 30.19%, as shown in Figure 6(f), and the THD value of source current in feeder-2 is 1.08%, as shown in Figure 6(g). Figure 7 (in Appendix) shows the simulation results of the UVCR-controlled proposed 5-level series RSMLI-2 of MD-UPQC in feeder-2 for voltage sags-swells and voltage harmonic distortions in load voltage. The source voltage consists of uneven harmonic distortions affecting the smooth operation of other loads interfaced at the PCC or end-user level. These harmonic distortions in source voltage are compensated by using 5-level RSMLI-2 of MD-UPQC device functioning in in-phase compensation mode.

The source terminal voltage is preserved as sinusoidal during the pre-harmonic condition, but it is distorted due to the existence of unequal 5th and 7th-order voltage harmonics in a period of 0.5 to 0.6 sec, as illustrated in Figures 7(a)-(e). During this time, MD-UPQC's 5-level series RSMLI-2 counteracts harmonic distortions in load voltage and keeps it harmonic-free, sinusoidal, and fundamental up to 340 V. During the pre-sag state, the source terminal voltage is balanced; however, due to the existence of voltage-sag, the source terminal voltage is dropped with a voltage of 170 V in a period of 0.15 to 0.25 sec. During this time, MD-UPQC's 5-level series RSMLI-2 injects the needed voltage of 170 V to keep the load voltage constant at 340 V and drive the non-linear load. During the pre-swell state, the source terminal voltage is balanced; however, due to the existence of voltage-swell, the source terminal voltage is increased with a voltage of 510 V in a period of 0.35 to 0.45 sec. During this time, MD-UPQC's 5-level series RSMLI-2 extracts an additional voltage of 170 V to keep the load voltage constant at 340 V and drive the non-linear load. However, it improves the load voltage, reactive power, and power factor in feeder-2 to make system characteristics balanced, sinusoidal, linear, and fundamental. According to IEEE-519/1992 standards, the THD value of source voltage in feeder-2 during harmonic period is determined as 20.62% and the THD value of load voltage in feeder-2 during harmonic correction is calculated as 0.36%.

3.2. Performance of UVCR-controlled proposed 5-level RSMLI-MDUPQC device for mitigation of voltage allied PQ issues in feeder-1

Figures 8, especially Figures 8(a)-(e) (in Appendix) shows the simulation results of UVCR-controlled proposed 5-level series RSMLI-3 of MD-UPQC in feeder-1 for mitigation of voltage sags-swells, voltage deviations, and voltage harmonic distortions in load voltage of 50 Hz power supply. The source voltage has unequal harmonic distortions that impact the smooth functioning of other loads interfaced at the PCC or end-user level. These harmonic distortions in source voltage are adjusted by utilizing the MD-UPQC device's 5-level RSMLI-3 in in-phase compensation mode. During the pre-harmonic state, the source terminal voltage remains sinusoidal, but it is distorted due to the presence of unequal 5th and 7th-order voltage harmonics in a period of 0.6 to 0.7 sec. During this time, MD-UPQC's 5-level series RSMLI-3 counteracts harmonic distortions in load voltage and maintains a harmonic-free, sinusoidal, and fundamental voltage of 340 V. During the pre-sag state, the source terminal voltage is balanced; however, owing to the existence of voltage-sag, the source terminal voltage is dropped with a voltage of 170 V in a period of 0.2 to 0.3 sec. During this time, the MD-UPQC 5-level series RSMLI-3 injects the needed voltage of 170 V to keep the load voltage constant at 340 V. During the pre-swell state, the source terminal voltage is balanced; however, due to the existence of voltage-swell in the period of 0.4 to 0.5 sec, the source terminal voltage is raised with a value of 510 V. During this time, MD-UPQC's 5-level series RSMLI-3 extracts an additional voltage of 170 V to keep the load voltage constant at 340 V. During pre-voltage deviations, the source terminal voltage remains balanced; however, owing to the existence of voltage-deviations, the source terminal voltage is reduced to 0 V in a period of 0.75 to 0.85 sec. During this time, the MD-UPQC 5-level series RSMLI-3 injects the full-rated voltage of 340 V to keep the load voltage constant at 340 V and drive the crucial load. However, it increases the load voltage, reactive power, and power factor in feeder-1 to make system characteristics balanced, sinusoidal, linear, and fundamental. According to IEEE-519/1992 standards, the THD value of source voltage in feeder-1 during harmonic period is estimated as 20.62%, as shown in

Figure 8(d), and the THD value of load voltage in feeder-1 during harmonic compensation is calculated as 0.52%, as shown in Figure 8(e).

The performance of the 5-level RSMLI topology-based MD-UPQC device is shown in Figure 9 (in Appendix). It includes Figure 9(a) shows the output voltage of 5-level RSMLI topology, Figure 9(b) shows the THD value of the output voltage of RSMLI topology, and Figure 9(c) shows common DC-Link voltage, respectively. The 5-level staircase AC output voltage reduces the dv/dt and di/dt, low common-mode voltage, low peak-current ratings, low electro-magnetic loss, and high efficiency. The 5-level output voltage of RSMLI topology is measured as a constant of 1320 V and the THD value of 5-level output voltage is calculated as 24.78%, it enhances the THD value of traditional VSI and DCMLI topology and requires low-burden filter units for producing sinusoidal voltage wave-shape. The common DC-link voltage across the DC capacitor is retained as a constant of 1320 V and is regulated by using an inbuilt DC voltage controller in the UVCR control scheme. The comparisons of source, critical load, and RSMLI output voltage THDs of traditional and proposed compensation devices in feeder-1 and feeder-2 are illustrated in Table 3.

Table 4 shows a comparison of the source, non-linear load current THDs of existing and suggested correction devices in feeder-2. Table 5 compares the necessary switching components of basic MLIs and suggested RSMLI topologies for 5-level voltage at load terminals. Compared to basic MLI and standard RSMLI topologies, the suggested 5-level RSMLI topology requires just four switches and a single DC source, reducing topology size, cost, and complexity.

Table 3. Comparisons of source, critical load, RSMLI output voltage THDs of traditional and proposed compensation devices in feeder-1 and feeder-2

THD (%)	Source voltage	Load voltage		Output voltage (%)
		Feeder-1 (%)	Feeder-1 (%)	
Traditional 3-level VSI Based MD-UPQC [20]	20.62%	1.84	1.72	91.7
Traditional 5-level DCMLI MD-UPQC [21]		0.89	0.54	27.5
Proposed 5-level RSMLI Based MD-UPQC		0.52	0.36	24.78

Table 4. Comparisons of source, non-linear load current THD of traditional and proposed compensation devices in feeder-2

THD (%)	Source current (%)	Non-linear load current (%)
Traditional 3-level VSI Based MD-UPQC [20]	5.12	30.14
Traditional 5-level DCMLI Based MD-UPQC [21]	1.47	30.19
Proposed 5-level DCMLI Based MD-UPQC	1.08	30.18

Table 5. Comparison of required switching elements of traditional and proposed RSMLI topologies for 5-level output voltage

	Basic MLI topologies			Reduced-switch MLI topologies		
	DCMLI [13]	FCMLI [14]	CHMLI [15]	6-Switch RSMLI [17]	5-Switch RSMLI [18]	Proposed RSMLI
Switches	8	8	8	6	5	4
Clamping diode	12	0	0	0	0	0
Balancingcapacitors	0	6	0	0	0	0
DC voltage sources	2	2	2	2	2	1
Gate-drive circuits	8	8	8	6	5	4

4. CONCLUSION

The effectiveness of the proposed five-level RSMLI topology of MD-UPQC is dependent on its enhanced capacity to provide the necessary compensation currents/voltages in response to various PQ issues. Additionally, this topology ensures the uninterrupted flow of power between the feeders. The proposed novel 5-level RSMLI topology with reduced switch count addresses several technical and economic challenges present in traditional 3-level VSIs and DCMLI topologies. The novel RSMLI topology, as proposed, necessitates a mere four switches, a single DC source, and uniform gate-drive circuits to produce a five-level output voltage. This configuration effectively diminishes the dimensions, expenses, and intricacy associated with MLI modules when compared to conventional MLI topologies. The UVCR control method is distinguished by its use of simplified mathematical analysis and ability to minimize computational latency in processing reference current/voltage data for controlling the 5-level RSMLI-MDUPQC device. The suggested topology's performance, UVCR-controlled 5-level RSMLI-MDUPQC, is validated using the computational tool MATLAB-Simulink. Following that, the simulation results are shown. To achieve

effective compensation characteristics, the THD values of the source currents and load voltages comply with the IEEE-519/1992 standards.

APPENDIX

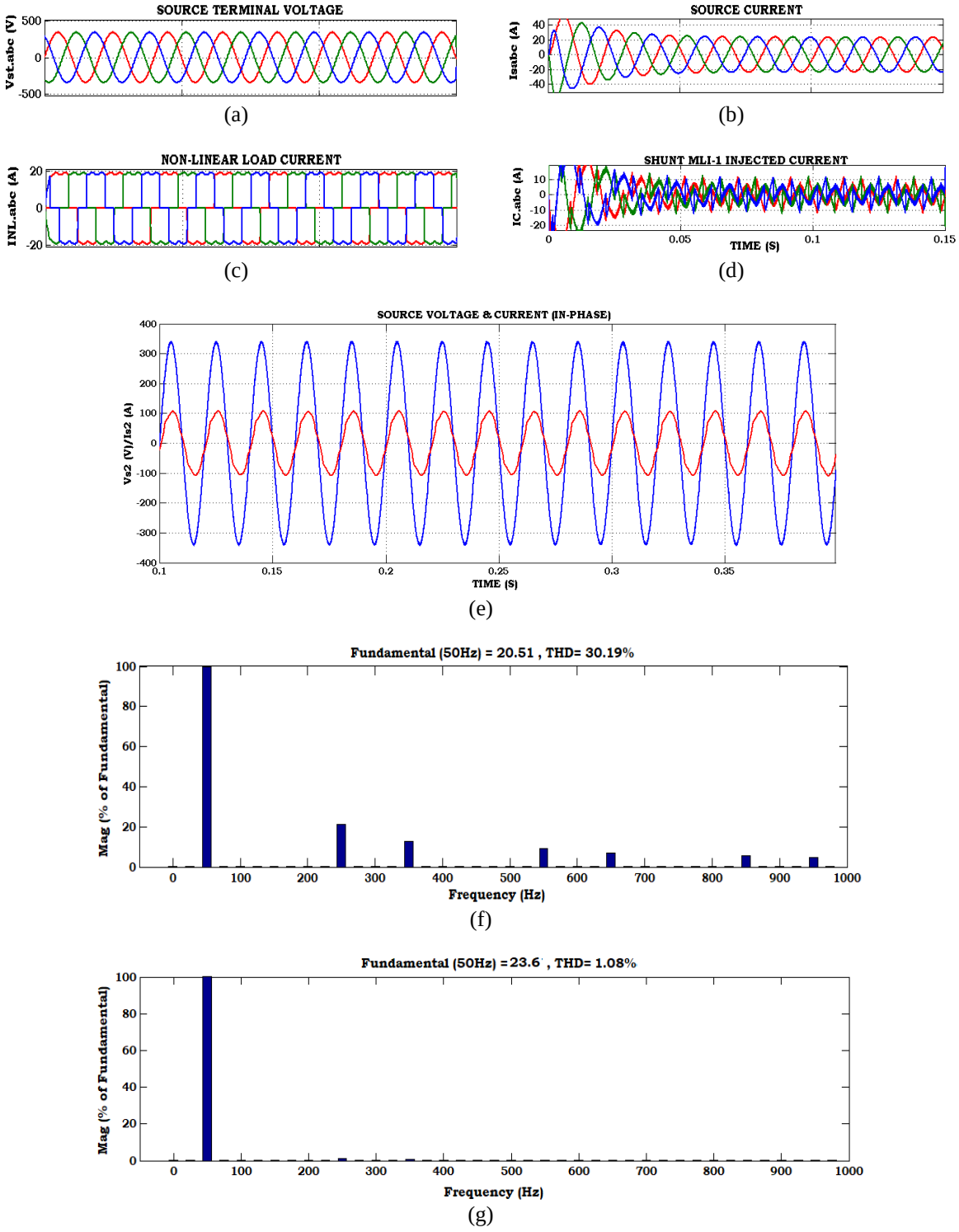


Figure 6. Simulation results of UVCR controlled proposed 5-level shunt RSMLI-1 of MD-UPQC device in feeder-2: (a) source terminal voltage, (b) source current, (c) non-linear load current, (d) shunt RSMLI-1 injected current, (e) source current in-phase with source voltage, (f) THD of non-linear load current in feeder-2, and (g) THD of source current in feeder-2

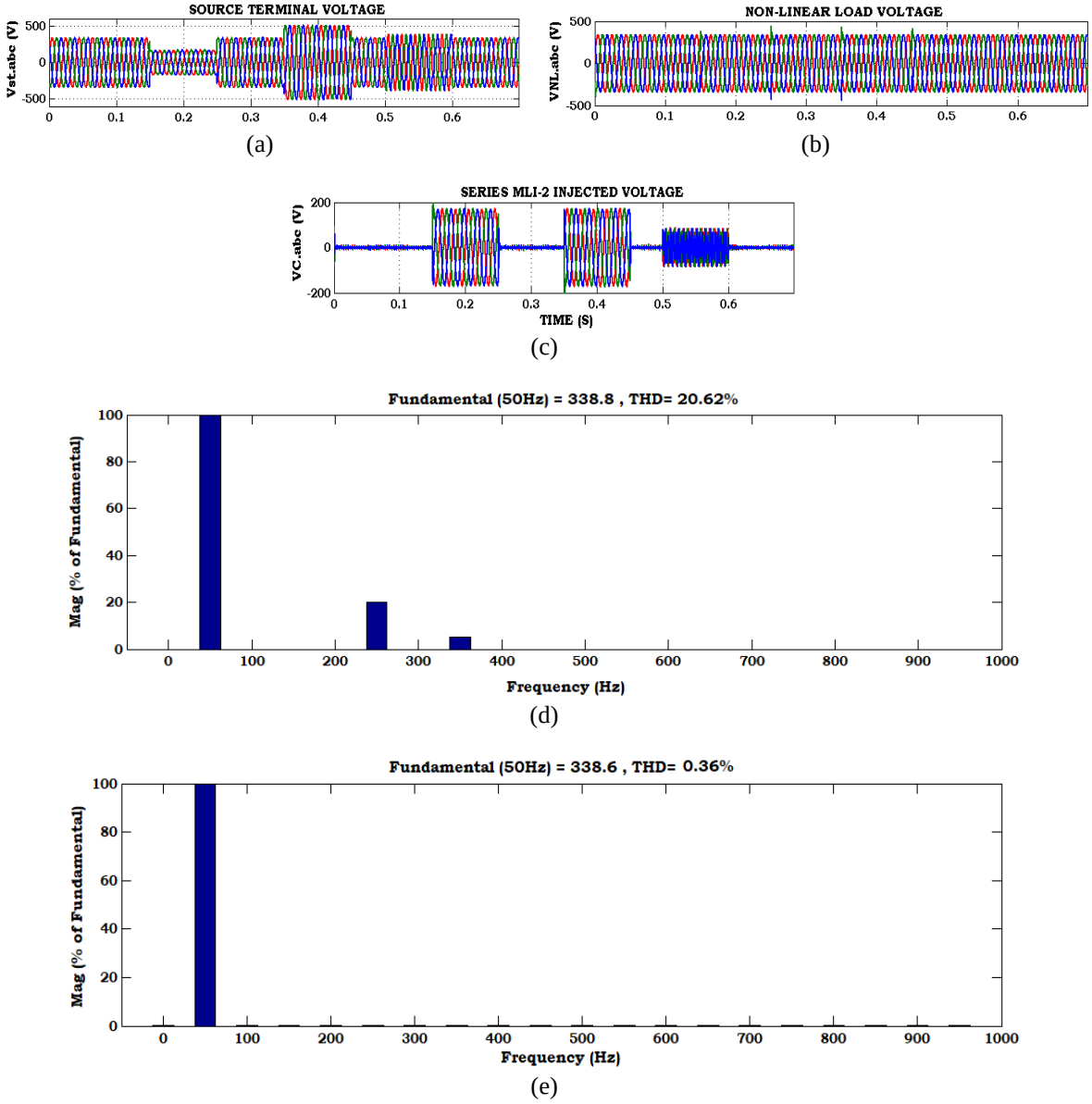
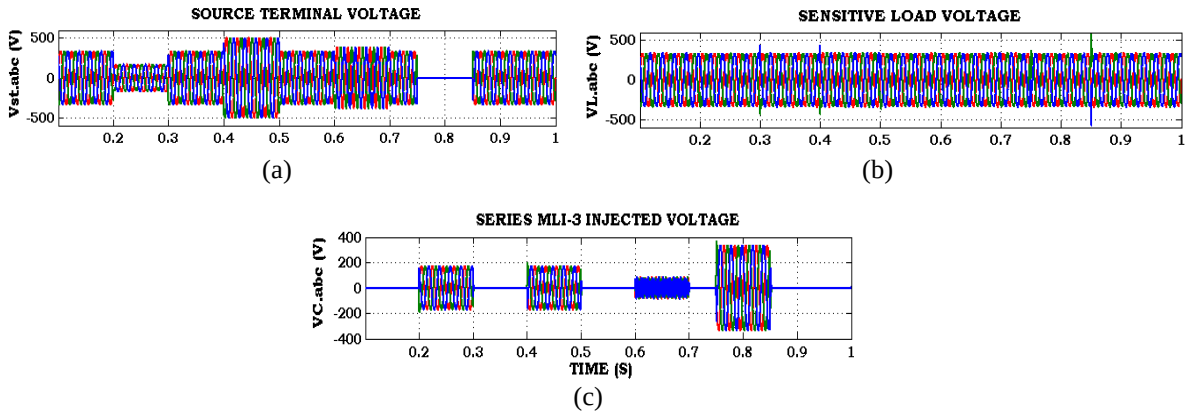
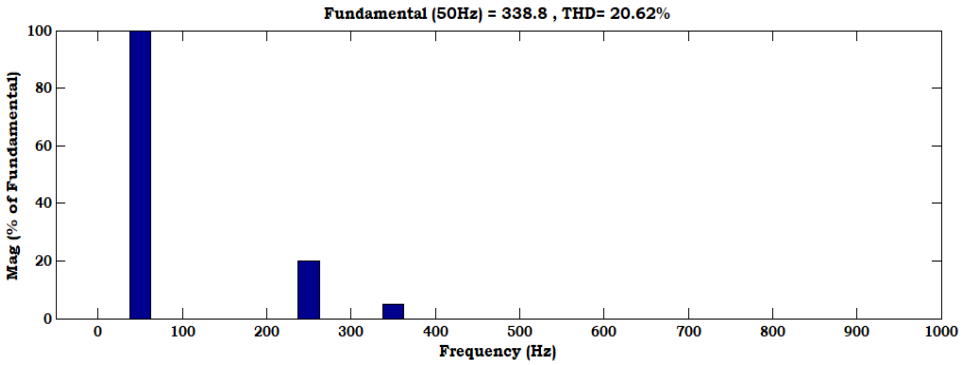
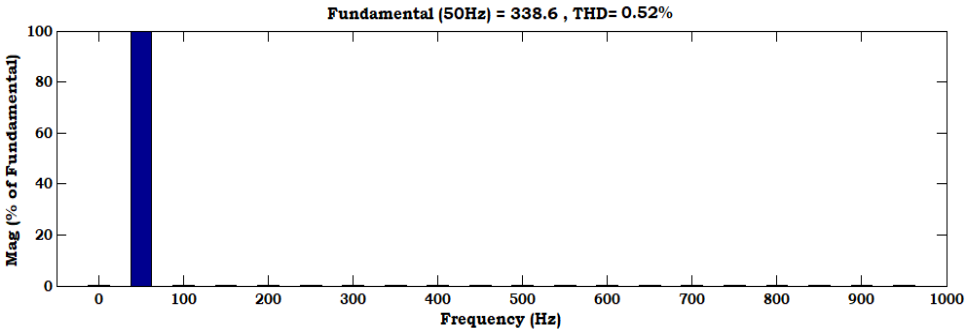


Figure 7. Simulation results of UVCR controlled proposed 5-level series RSMLI-2 of MD-UPQC device in feeder-2: (a) source voltage, (b) load voltage, (c) series RSMLI-2 injected voltage, (d) THD of source voltage in feeder-2, and (e) THD of non-linear load voltage in feeder-2



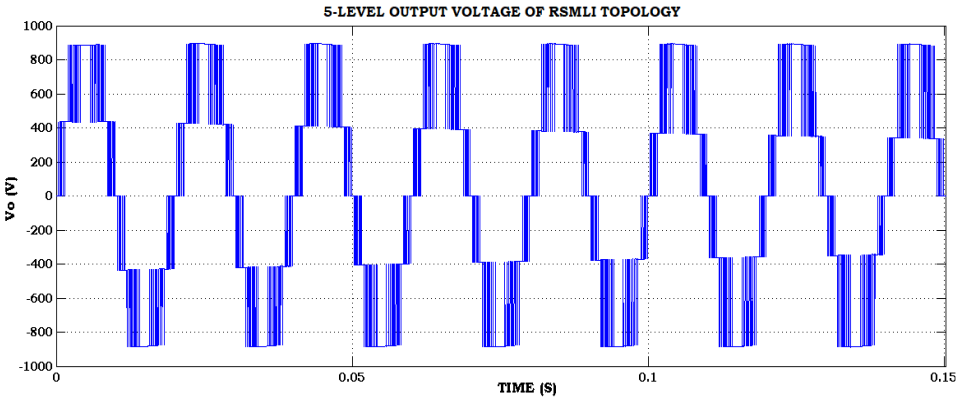


(d)

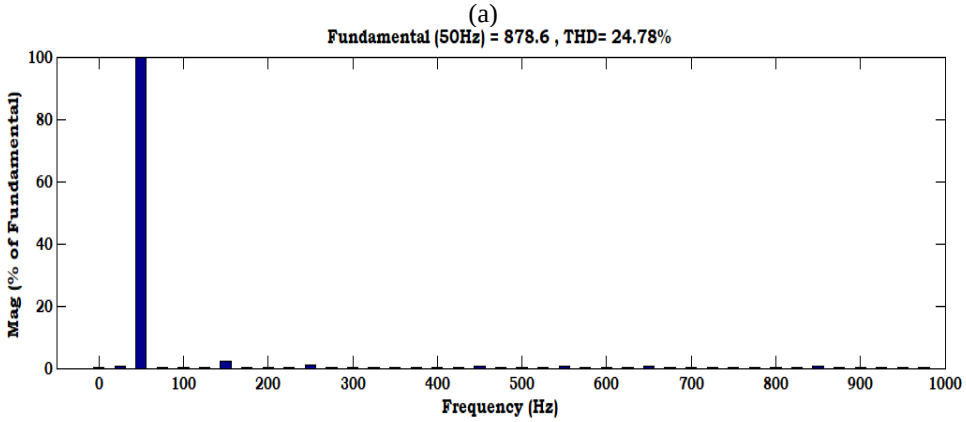


(e)

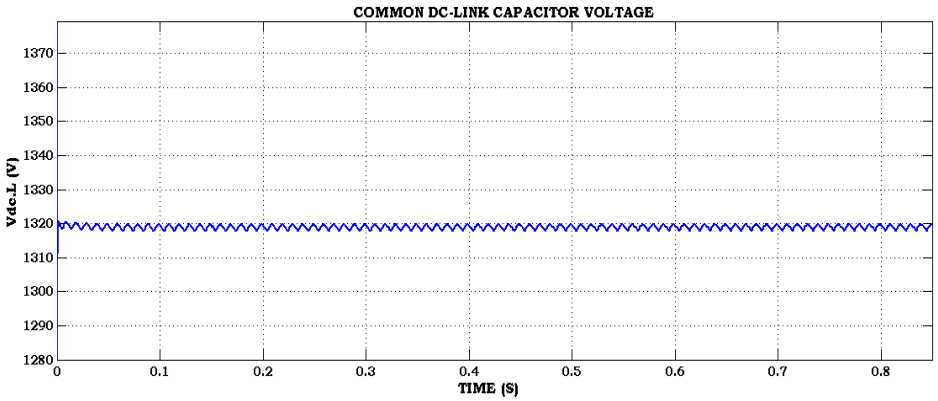
Figure 8. Simulation results of UVCR controlled proposed 5-level series RSMLI-3 of MD-UPQC device in feeder-1: (a) source terminal voltage, (b) sensitive load voltage, (c) series RSMLI-3 injected voltage, (d) THD of source voltage in feeder-1, and (e) THD of critical load voltage



(a)



(b)



(c)

Figure 9. Performance of 5-Level RSMLI topology: (a) output voltage of 5-level RSMLI topology, (b) THD value of output voltage of RSMLI topology, and (c) common DC-link voltage

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