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CHBMLI based DSTATCOM for power quality improvemt in a three-phase three-wire distribution system with PI controller

Thiruveedula Madhu Babu[1], Kalagotla Chenchireddy[2], Kama Sreevarsha[1], Badudhala Praveen[1], Mohammad Thanveer[1], Ganji Kashinadh[1]
[1]Department of Electrical and Electronics Engineering, Teegala Krishna Reddy Engineering College, Hyderabad, India
[2]Department of Electrical and Electronics Engineering, Geetanjali College of Engineering and Technology, Hyderabad, India

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ABSTRACT

This paper presents a cascaded h-bridge (CHB) multilevel inverter (MLI) based MLI based distribution static synchronous compensator (DSTATCOM). The main objective of this paper is to reduce source current harmonics in the distribution system by using a cascade H-bridge multilevel inverter (CHBMLI) as DSTATCOM with a proportional-integral (PI) controller. The PI controller compensates reactive power, reduces source current harmonics, and maintains the unity power factor in the distribution system. The conventional two-level inverter-based DSTATCOM has many disadvantages such as high total harmonic distortion (THD), and high switching stress power semi-conductor devices, suitable for only low-power applications. This paper to overcome these drawbacks by using MLI-based DSTATCOM. The proposed system simulations are verified in MATLAB/Simulink software. The verified results are source current, load current, and compensating current.

Corresponding Author:

Thiruveedula Madhu Babu
Department of Electrical and Electronics Engineering, Teegala Krishna Reddy Engineering College
Medbowli, Meerpet, Saroornagar, Hyderabad–500097, Telangana, India
Email: madhumk448@gmail.com

1. INTRODUCTION

In particular, a five-level voltage inverter with an H-bridge topology is the subject of the study's analysis of energy indicators for multilevel voltage converters. The rising demand for energy-efficient technological processes, power-efficient semi-conductor converters, and accurate reactive power level regulation fuels the importance of the study. Two-stage, three-phase circuits coupled in a wye configuration are used by the inverter in question [1]. In this work, a brand-new converter design for tying three-phase photovoltaic (PV) panels to the grid is presented. The converter uses a distinctive topology in the five-level class and only a few power semiconductor switches. The solar source, a two-phase inverter, and a Scott-t transformer that transforms the inverter's two-phase output into three phases for grid connection make up the converter's three primary components [2]. In this research, a novel method for a three-phase, five-level multilevel inverter (MLI) with a five-level output voltage is presented. Traditionally, a three-phase full-bridge circuit and an extra bidirectional switch have been employed to achieve the 5-level output voltage by splitting a direct current (DC) voltage source using two capacitors. However, this strategy has produced issues including capacitor voltage imbalances and output voltage restrictions [3]. The switching angles of three-phase five-level cascade H-bridge MLI with unknown switching angles are introduced in this research using a novel way. The selective harmonic elimination pulse width modulation (PWM) approach is used across a wide range of modulation indices to improve total harmonic distortion (THD). The idea entails connecting two

of these inverter modules in series with switched-capacitor units (SCUs) that are 2L in size [4]. By adjusting the output current of the DC bus, this technique aims to provide an inverter output that has five levels.

The method is based on the modulation scheme of a current source inverter with five levels. This approach modifies the switching state of the inverter as well as the DC bus current using logical transformations. As a result, it makes it possible for the current source inverter to provide a five-level output without needing more [5], [6]. The problem of harmonics in solar PVenergy conversion systems, which can impair power quality, is discussed in this work. Proportional integral (PI), artificial neural network (ANN), and fuzzy logic (FL) controllers are three alternative controller systems that are used to reduce harmonics in a solar-powered cascaded fifteen-level inverter [7]. The unified power quality conditioner (UPQC), an MLI-based cascaded H-bridge (CHB) solution, is presented in the study as a novel approach to resolving various power quality problems. These issues include reactive power compensation, current unbalance, reactive power harmonics, voltage harmonics, and voltage sag. Six H-bridges and three DC link capacitors are used in the proposed method's three-level UPQC [8]–[10]. The UPQC is described in the study as a vital tool for improving power qualityin a power system. The research focuses on a reduced switch MLI that is managed by a soft computing ANN. Several power quality issues, such as voltage sag, voltage swell, power factor, harmonics, and voltage compensation restoration time are intended to be mitigated by this new configuration [11], [12]. The UPQC, a significant power conditioner designed to enhance power quality for consumers and utility points, is discussed in the paper's discussion of the importance of power systems. A five-level output produced by the UPQC's series and shunt controllers is filtered to provide compensatory signals. The voltage and current profiles in the power distribution system areimproved by these signals [13]–[15]. To comply with utility grid power quality standards for harmonic currents and voltages, the article discusses the requirement for active power filters in contemporary power systems. For both balanced and unbalanced nonlinear loads, the emphasis is on lowering THD in source currents and correcting for reactive power. The article introduces a shunt active power filter (SAPF), a 3-phase 5-level CHB-based multi-level inverter (MLI), to do this [1], [16]–[19].

2. DSTATCOM

Figure 1 shows the distribution static synchronous compensator (DSTATCOM) topology. A DSTATCOM stands for distribution static compensator. It is a type of power electronic device used in the field of electrical power distribution and quality control [20]–[24]. A DSTATCOM is designed to improve the quality of electrical power in distribution systems by mitigating power quality issues such as voltage sag, voltage swell, flicker, and harmonics. It can also provide reactive power compensation.

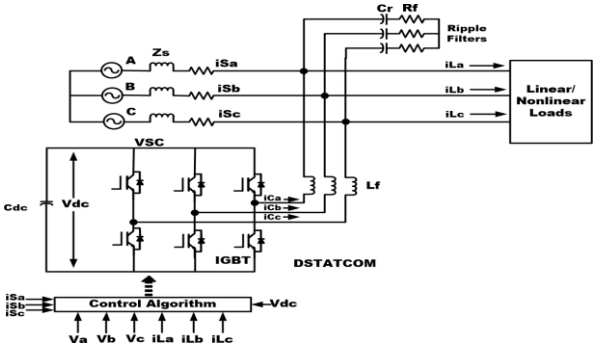


Figure 1. DSTATCOM topology

2.1. Proposed DSTATCOM topology

Figure 2 shows the proposed DSTATCOM topology. A 5-level inverter using a CHB and PI Controller to improve power quality in the distribution system is shown in the Figure 2. A 3-phase 5-level inverter in the system directs a 3-phase supply with R, Y, and B phases to a non-linear load. There are two capacitors and eight switches in this inverter. An inductor connects the inverter to the power supply's two separate phases. insulated-gate bipolar transistors (IGBT) are used in the switches, and they each have a parallel-connected diode. To provide a voltage rating greater than the IGBT reverse-blocking voltages, the IGBT modules are connected in series. The voltage of the capacitor Vdca1 must be half or less of the required voltage level. Filter reactors, often referred to as La, Lb, and Lc inductors, are used to remove undesirable

harmonics from the three-phase electric power system or transmission line. The single phase (R) through a filter reactor (La) serves as the source of power for the multi-level inverter. To control larger voltage ratings, the IGBTs are connected in series. The IGBT's switching pattern determines how and when the capacitor charges and discharges. When switches Sa11, Sa12, Sa24, and Sa23 are ON, capacitorsdischarge continually, and the alternation of charging and discharging balances the voltage of the capacitors. To do this, sensor-less voltage balancing is combined with sinusoidal pulse width modulation with level shifting. Voltages from capacitors are gathered, sent to the Y-phase, and repeated for the other connections. When gathered, the capacitor voltages are applied to a non-linear load to reduce THD.

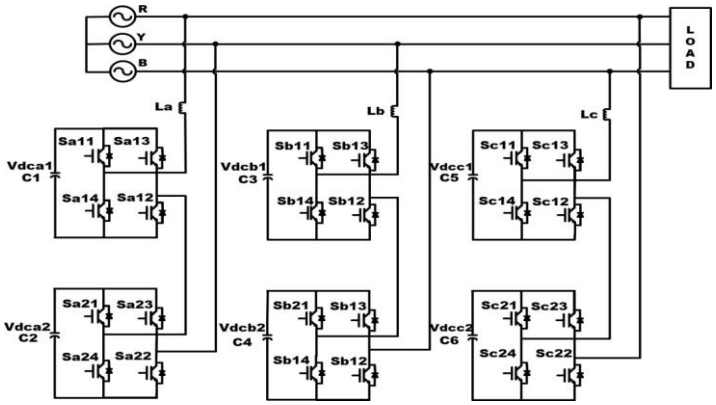


Figure 2. Proposed DSTATCOM topology

3. SYNCHRONOUS REFERENCE FRAME THEORY

Figure 3 shows the synchronous reference frame theory. The voltage at the point of common coupling [PCC] or PCC (Vs) is transformed to the rotating reference frameas a result of the ABC-do conversion utilizing Park's transformation. Low-pass filters (LPFs) remove oscillatory and harmonic components from voltages. The following is how PCC determines the load voltage's [VL] amplitude:

$$\begin{aligned} V_a &= V_m\, Sin\,(wt) \\ V_a &= V_m\, Sin\left(wt - \tfrac{2\pi}{3}\right) \\ V_c &= V_m\, Sin\left(wt - \tfrac{4\pi}{3}\right) \end{aligned} \tag{1}$$

$$\begin{aligned} i_{La} &= \sum I_{Lan}\, Sin\{n(wt) - \theta_{an}\} \\ i_{Lb} &= \sum I_{Lbn} sin\left\{n\left(wt - \tfrac{2\pi}{3}\right) - \theta_{bn}\right\} \\ i_{lc} &= \sum I_{Lcn} Sin\left\{n\left(wt - \tfrac{2\pi}{3}\right) - \theta_{cn}\right\} \end{aligned} \tag{2}$$

$$\begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} = \sqrt{\tfrac{2}{3}} \begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3/2} & -\sqrt{3/2} \end{bmatrix} \begin{bmatrix} i_{La} \\ i_{Lb} \\ i_{Lc} \end{bmatrix} \tag{3}$$

$$\begin{bmatrix} i_d \\ i_q \end{bmatrix} = \begin{bmatrix} \cos\theta & \sin\theta \\ -\sin\theta & \cos\theta \end{bmatrix} \begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} \tag{4}$$

$$\begin{bmatrix} i_{\alpha dc} \\ i_{\beta qc} \end{bmatrix} = \begin{bmatrix} cos\,\theta & sin\,\theta \\ -sin\,\theta & cos\,\theta \end{bmatrix} \begin{bmatrix} i_{ddc} \\ i_{qdc} \end{bmatrix} \tag{5}$$

$$\begin{bmatrix} i_{sa}^* \\ i_{sb}^* \\ i_{sc}^* \end{bmatrix} = \sqrt{\tfrac{2}{3}} \begin{bmatrix} \frac{1}{\sqrt{2}} & 1 & 0 \\ \frac{1}{\sqrt{2}} & -\frac{1}{2} & \frac{\sqrt{3}}{2} \\ \frac{1}{\sqrt{2}} & -\frac{1}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} i_0^* \\ i_{\alpha dc}^* \\ i_{\beta dc}^* \end{bmatrix} \tag{6}$$

The reference load voltages (V*La, V*Lb, V*Lc) in the ABC frame arc were obtained from the reverse park's transformation. The errors between the sensed load voltages (VLa, VLb, VLc) and reference load voltages are used in the PWM controller to generate gate pulses for the VSc. SRF theory is mainly used for extracting reference current. SRF theory measured phase angle and magnitude.

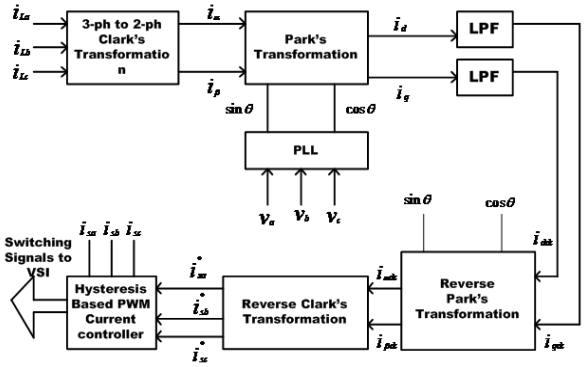


Figure 3. Synchronous reference frame theory

4. RESULTS AND DISCUSSION

The simulation results of three-phase three-wire DSTATCOM Results are presented in this section. Table 1 shows the simulation results table. Figure 4 shows the source voltage waveform in the distribution system. The source voltage waveform is pure sine wave. Figure 5 shows the load current waveforms, the load current has tripled harmonics. Figure 6 shows the source current waveform, the source current waveform highly distorted 0 to 0.01 sec the magnitude of the current doubles the fundamental current, the DSTATCOM compensated harmonics and maintained sine waveform. The Figure shows the DC link capacitor voltage waveforms of the first leg. Figure 7(a) shows the Leg-A capacitor one voltage and Figure 7(b) shows the Leg-A capacitor two voltage. Figure 8 shows the all-single-phase current waveforms. Figure 8(a) shows the source voltage, Figure 8(b) shows the source current, Figure 8(c) shows the compensating current, and Figure 8(d) shows the load current waveform. Figure 9 shows the THD waveform. Figure 9(a) source current and Figure 9(b) source current THD. The THD value is 4.95%. Figure 10 shows the experimental results of DSTATCOM with steady-state conditions. Figure 10(a) shows the source voltage, Figure 10(b) shows the source current, Figure 10(c) shows the load current waveform, and Figure 10(d) shows the compensating current.

Table 1. Simulation results

S.L.	Criteria	Achievement
1	Source voltage	230 V
2	Source Current	100 A
3	Load current	50 A
4	Dc link voltage	500 V
5	Switching frequency	100 kHz

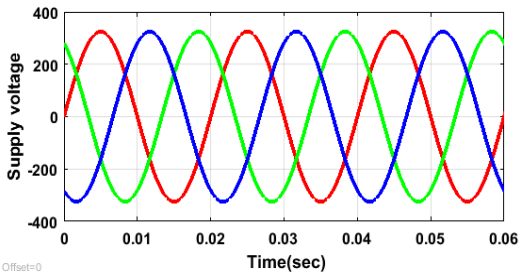


Figure 4. Three-phase source voltage

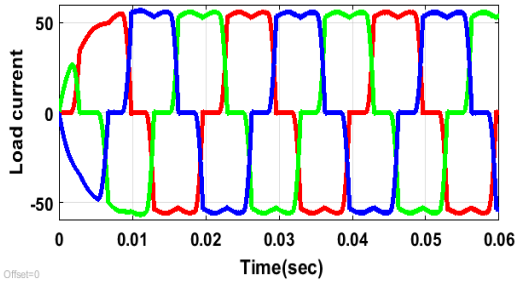


Figure 5. Three-phase load current

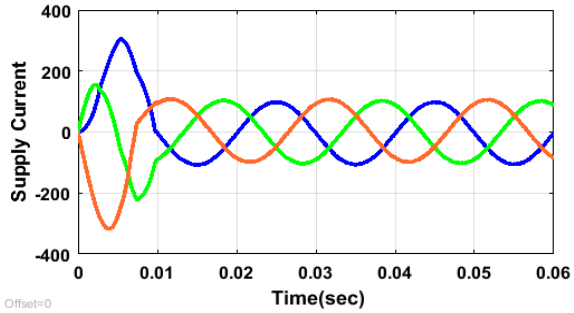
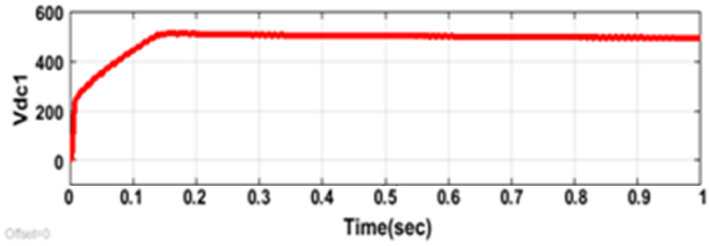
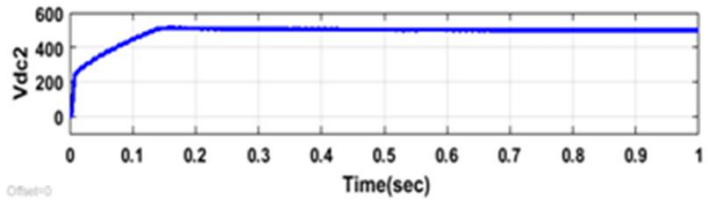


Figure 6. Three-phase source current

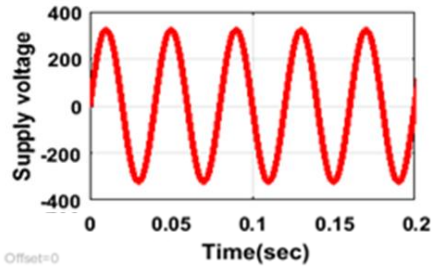


(a)

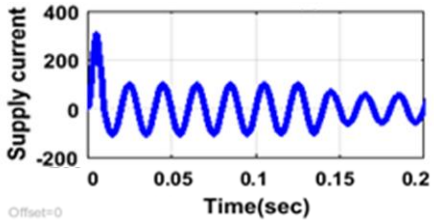


(b)

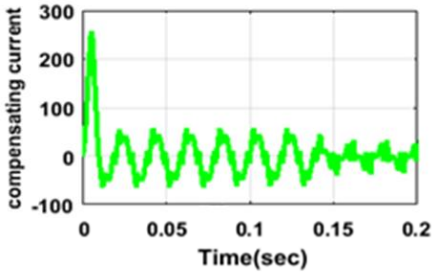
Figure7. DC link capacitor voltages for Leg-A capacitor in (a) one voltage and (b) two voltages



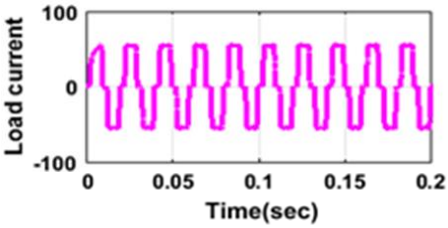
(a)



(b)

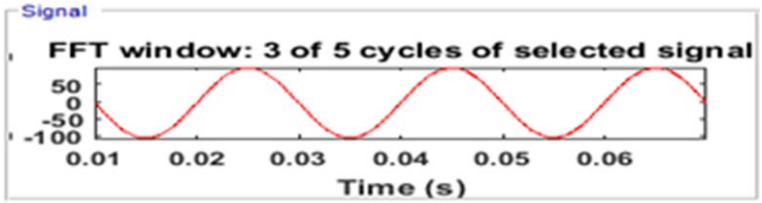


(c)

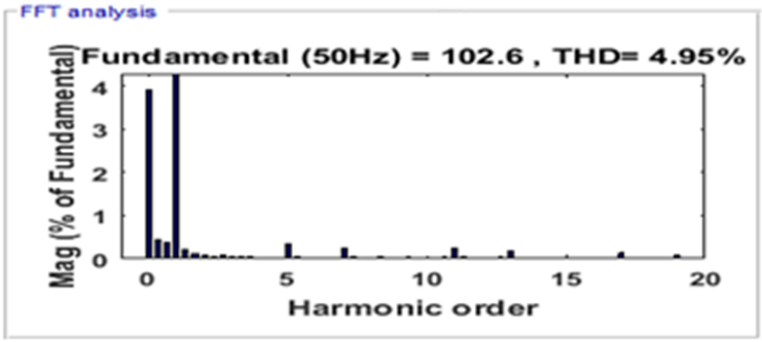


(d)

Figure8. Simulation waveforms of DSTATCOM in (a) single phase source voltage, (b) source current, (c) compensating current, and (d) load current

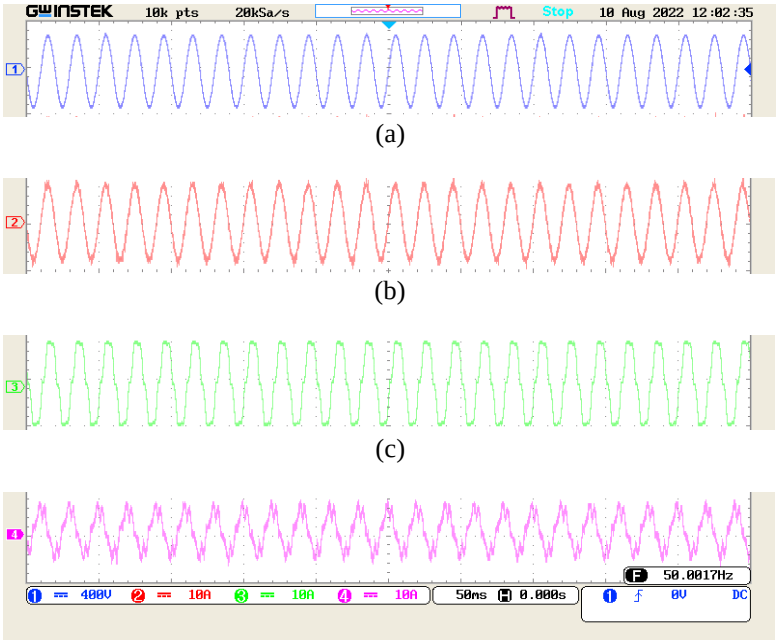


(a)



(b)

Figure 9. Source current THD waveform in (a) source current and (b) source current THD



(a)

(b)

(c)

(d)

Figure 10. Hardware results of DSTATCOM in (a) single phase source voltage, (b) source current, (c) compensating current, and (d) load current

5. CONCLUSION

This paper presents CHBMLI-based DSTATCOM. The proposed topology improved power quality in the distortion system. The proposed topology is controlled by the PI controller. The proposed system simulations are verified in MATLAB/Simulink software. The verified results are source current, load current, and compensating current. The experimental results are verified in OPAL-RT. The steady-state results are verified in real-time. This paper outcome reactive power compensation, source current harmonics elimination, and maintain unity power factor.

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BIOGRAPHIES OF AUTHORS

Thiruveedula Madhu Babu is received a B.Tech. from JNTU Hyderabad, Hyderabad, India, in 2010 and an M-tech from NIT Calicut 2012 respectively, and pursuing a Ph.D. in Annamalai University, India. He is working presently as an Assistant Professor and HOD at Teegala Krishna Reddy Engineering College, Hyderabad, India. He has presented technical papers in various national and international journals and conferences. He can be contacted at email: madhumk448@gmail.com.

Kalagotla Chenchireddy is received a B.Tech. and M.tech. from JNTU Hyderabad, Hyderabad, India, in 2011 and 2013 respectively, and pursuing Ph.D. in Karunya Institute of Technology and Sciences, Karunyanagar, Coimbatore, TN, India. He is working presently as an Assistant Professor at, Geethanjali College of Engineering and Technology, Keesara Mandal, Hyderabad, Telangana, INDIA. He has presented technical papers at various national and international conferences. His areas of interest include power electronics, power quality, and multilevel inverters. He is a regular reviewer of ISA Transactions, Cybernetics and Systems SCIE journals, IJPEDS, and IJAPE Scopus journals. He can be contacted at email: chenchireddy.kalagotla@gmail.com.

Kama Sreevarsha is presently a UG student in Electrical and Electronics Engineering, at Teegala Krishna Reddy Engineering College, Hyderabad, India. She has presented technical papers at various International Conferences. His areas of interest include power electronics, power quality, and multilevel inverters. She developed a single-phase inverter at Teegala Krishna Reddy Engineering College, Hyderabad. She can be contacted by email: sreevarshakama@gmail.com.

Badudhala Praveen is presently a UG student in the Electrical and Electronics Engineering Department, at Teegala Krishna Reddy Engineering College, Hyderabad, India. He has presented technical papers at various national and international conferences. His areas of interest include power electronics, power quality, and multilevel inverters. He can be contacted at email: bpraveen63033@gmail.com.

Mohammad Thanveer, is presently a UG Student in the Electrical and Electronics Engineering Department, at Teegala Krishna Reddy Engineering College, Hyderabad, India. He has presented technical papers at various National and International Conferences. His areas of interest include Power Electronics, Power quality; and Multilevel inverters. He can be contacted at email: thaneermohammad143@gmail.com.

Ganji Kashinadh he is presently UG Student in Electrical and Electronics Engineering Department, Teegala Krishna Reddy Engineering College, Hyderabad, India. . He has presented technical papers in various National and International Conferences. His area of interest includes Power Electronics, Power quality; Multilevel inverters. He can be contacted at email: kashiganji02@gmail.com.