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Fuzzy logic controller-based protection of direct current bus using solid-state direct current breaker

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ABSTRACT

Low-voltage direct current (LVDC) microgrids are increasingly utilized due to their efficiency and compatibility with distributed energy resources (DERs) and direct current (DC) loads, eliminating the need for multiple energy conversions. However, the protection of LVDC systems presents significant challenges, including high fault currents and the vulnerability of electronic devices. Traditional electromechanical circuit breakers are inadequate due to their slow response times. This work presents a protection approach for the DC bus in LVDC microgrids that combines a fuzzy logic controller (FLC) with a solid-state circuit breaker (SSCB). The FLC is designed to detect and respond to faults rapidly by processing input variables such as current magnitude and rate of change of current. The FLC controls the SSCB, which interrupts fault currents quickly and reliably. The proposed system demonstrates optimized fault-clearing times within milliseconds, significantly enhancing the protection and reliability of LVDC microgrids. This novel solution protects critical electronic components while also ensuring the microgrid's operational integrity. The FLC approach is utilized for optimizing fault-clearing duration within milliseconds.

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1. INTRODUCTION

Global energy consumption is becoming a more critical issue as technology expands worldwide. The developing energy systems must adapt to technological improvements, human needs, environmental concerns, and economic factors. As a result, it is critical to explore innovative strategies to ensure system security, ecological sustainability, power quality, generation costs, and transmission efficiency. The depletion of fossil fuel supplies, along with an increase in glasshouse gas emissions, has accelerated the development of alternative forms of integration of distributed generation, renewable energy sources (RES), and energy storage technologies. Microgrids can function autonomously from the main utility grid during natural disasters and power outages [1]–[5]. Direct current (DC) microgrids offer several advantages, including the effortless addition of DC sources and loads, the absence of reactive power correction, minimal synchronization issues, and the smooth addition of large-scale solar photovoltaic (PV) schemes. However, protecting DC microgrids is challenging due to the large size of DC currents that cause faults and the lack of experience with DC protection systems. To overcome this issue, solid-state circuit breakers (SSCBs) are used for protection since they can interrupt current in milliseconds, which is far quicker than electromechanical

circuit breakers. SSCBs are also more reliable and require less maintenance than electromechanical circuit breakers [6]–[10].

In addition, SSCB can be used to implement more progressive protection schemes, such as selective tripping and zone protection. These schemes can help to isolate faults and prevent damage to equipment. Overall, solid-state circuit breakers offer several advantages over electromechanical circuit breakers for the protection of DC microgrids. They are faster, more reliable, and more versatile. As a result, they are becoming the preferred choice for DC microgrid protection. Figure 1 shows a low-voltage direct current (LVDC) microgrid with three distributors and nine loads [11]–[15]. The loads are grouped into three sets, with each set of three loads connected in parallel to a distributor using programmable switches. The load types include motor, heater, and light load. Load ratings: voltage-48 V and capacity-500 W.

Figure 2 depicts a hybrid power system integrating an alternating current (AC) grid, PV array, battery bank, and a control circuit using fuzzy logic to manage DC loads. The AC grid supplies power to a 3-phase, 2-winding transformer configured in a Delta-Y_n (Delta-YN) arrangement. This transformer adjusts the voltage levels suitable for conversion. The transformed AC power is then fed into AC-DC converters, which convert it into DC power [16]–[20]. Parallel to this, a PV array coupled with a battery bank provides an alternative DC power source, ensuring energy availability even when the AC grid is unavailable. Both the converted DC power after the AC grid and the direct DC control from the PV array and battery bank are regulated by a control circuit employing a fuzzy logic controller (FLC). This control circuit optimizes the power flow and maintains a stable output for the DC loads, enhancing the system's reliability and efficiency. The combination of these components ensures a continuous and efficient power source to the DC loads, balancing energy sources from both the AC grid and renewable PV array while incorporating energy storage for reliability.

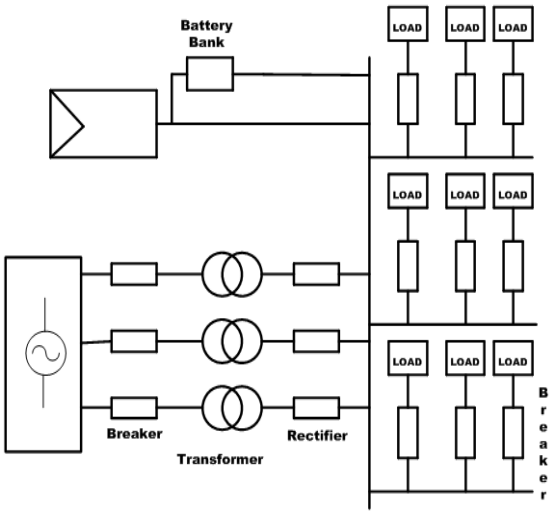


Figure 1. Block drawing of LVDC microgrid

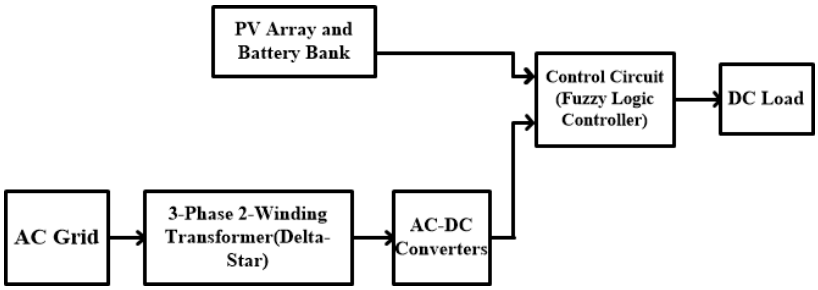


Figure 2. Block diagram of the proposed model

2. OPERATION OF SOLID-STATE CIRCUIT BREAKER WITH BI-DIRECTIONAL BLOCKER

A SSCB utilizes power metal-oxide-semiconductor field-effect transistors (MOSFETs) or insulated gate bipolar transistors (IGBTs) to control current movement in together instruction. Current and voltage

sensors continuously monitor the system, enabling real-time fault detection. In the event of an overcurrent, the control unit signals the gate drivers to immediately turn off the MOSFETs or IGBTs, effectively stopping the current flow [21]–[25]. Diodes are incorporated to accurately detect current direction and provide additional protection. Once the fault is cleared, the system can be reset either physically or mechanically. To enhance reliability, the breaker includes safeguards such as thermal protection and undervoltage lockout. Compared to conventional mechanical breakers, this solid-state design offers faster response, greater reliability, and increased durability. The diagram of the bi-directional SSCB is shown in Figure 3.

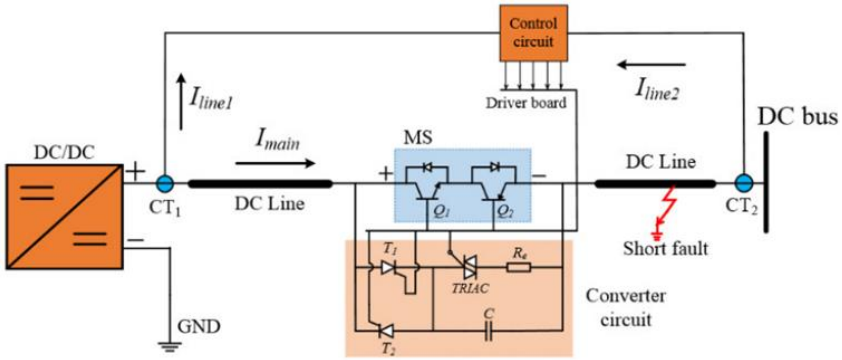


Figure 3. Schematic plan of a bi-directional fault with a current blocker

Figure 4 shows the construction of a bi-directional fault current blocker. Under normal operating conditions, the IGBTs remain bowed on, while the other components, such as silicon-controlled rectifiers (SCRs) and triode for alternating currents (TRIACs), are kept off, as illustrated in Figure 4(a). The DC bus is connected in series with the bi-directional solid-state circuit breaker (BSCCB), allowing the esteemed current to flow finished the two IGBTs and their reverse-parallel diode counterparts. The voltage drops across the IGBTs and diodes during conduction are minimal, resulting in a compact blocker design that does not delay with the normal process of other system components. In the event of a fault, the IGBTs are switched off, and thyristor T1 is activated, as shown in Figure 4(b). The liability current passes from the thyristor to the charging capacitor and then to the external circuit. The fault current gradually declines to zero. By gripping the fault current, the blocking capacitor is fully charged, then reducing the current through the thyristor to less than its holding current value and eventually turning it off, as illustrated in Figure 4(c). In the last stage, the circuit breaker returns to its regular working mode, switches on the IGBTs, and discharges the blocking capacitor as heat via a resistor (R_e), as illustrated in Figure 4(d). However, these two procedures do not interfere with one another.

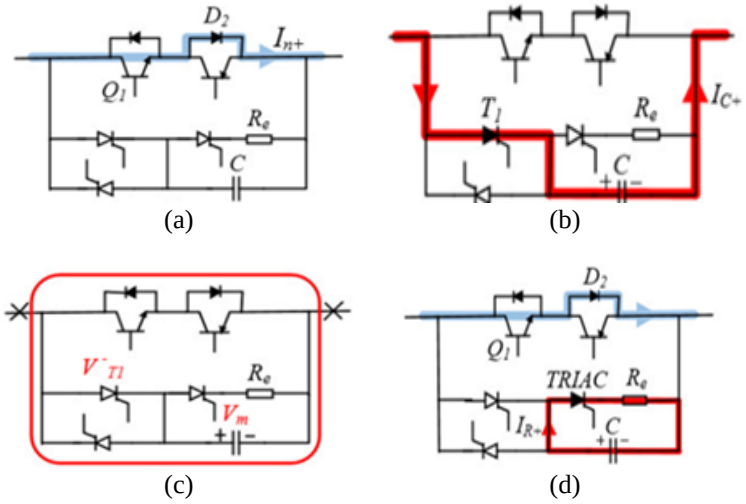


Figure 4. Construction of a bi-directional fault current blocker of (a) usual stage, (b) obstructive capacitor charging phase, (c) fault current delaying stage, and (d) reclosing and dump energy emancipating stage

3. FUZZY LOGIC CONTROLLER STRATEGY

The integration of an FLC with an SSCB enables intelligent protection of the DC bus, utilizing the benefits of adaptive control and rapid response to significantly enhance the reliability, efficiency, and fault tolerance of power systems. This paper implements an FLC to monitor and control DC bus operating conditions in real-time, utilizing linguistic variables and a rule-based system to process inputs such as current, voltage, and temperature, and then determines the appropriate action to protect the DC bus from faults or overloads. When a fault condition is detected, the FLC sends a control signal to the SSCB, which quickly interrupts the circuit to prevent damage. Unlike traditional mechanical breakers, SSCBs offer rapid switching capabilities, minimizing the interruption time and reducing the risk of arc flash and other hazards. The combination of FLC and SSCB ensures that the protection system is adaptive and robust, capable of handling a wide range of fault scenarios with high precision. This energy enhances the overall stability and safety of the DC power system, making it particularly suitable for applications in RES, electric vehicles, and other advanced power electronic applications. The design of the FLC categorizes both input and output variables into five linguistic terms: negative big (NB), negative small (NS), zero (ZE), positive small (PS), and positive big (PB). At each sampling interval, the system receives input variables based on the defined sampling time. Through the process of fuzzification, numerical inputs are converted into these linguistic terms using membership functions (MFs). After the initial theoretical design, the MFs and associated rules were fine-tuned to enhance performance and minimize errors.

The fuzzy inference system (FIS) processes the fuzzified input vector using a predefined set of fuzzy rules to determine the corresponding output vector. Table 1 illustrates the truth table representing system transitions based on its current state and the change in that state. Rows correspond to the current state, while columns represent potential changes; each cell indicates the resulting system state under a specific condition. With two input variables, each having five fuzzy sets (5^2), the FLC incorporates a total of 25 rules to cover various operating conditions, as detailed in the table. The supervisor is constructed using membership purposes for the input limits, such as the error (e) and the change in error Δe\Delta eΔe, as in (1)-(3).

$$P = P_{in}(k) = V_{in}(k) \times I_{in}(k) \tag{1}$$

$$error\ (e) = \left(\frac{P_{in}(k) - P_{in}(k-1)}{V_{in}(k) - V_{in}(k-1)}\right) \tag{2}$$

$$Change\ in\ error\ (\Delta e) = E(k) - E(k-1) \tag{3}$$

The MFs for the inputs and outputs of the FLC are illustrated in Figures 5 and 6.

Table 1. FLC rules table

Current/change in current	NB	NS	Z	PB	PS
NB	NB	NB	NS	NS	Z
NS	NB	NS	NS	Z	PS
Z	NS	NS	Z	PS	PS
PB	NS	Z	PS	PS	PB
PS	Z	PS	PS	PB	PB

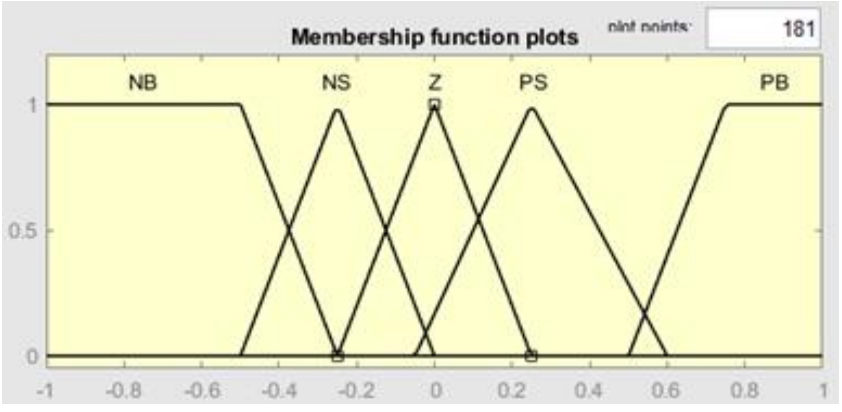


Figure 5. Inputs (e, Δ*e*)

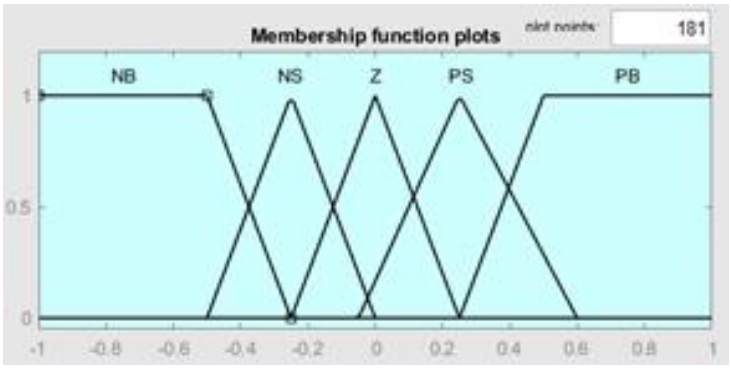


Figure 6. Output

4. FUZZY INFERENCE SYSTEM

FIS are broadly categorized into two types: Mamdani and Sugeno. While Sugeno FIS is typically limited to multiple-input, single-output systems, Mamdani FIS is versatile, supporting both multiple-input single-output (MISO) and multiple-input multiple-output (MIMO) configurations. Due to this flexibility, the Mamdani approach is adopted in this work. Mamdani-type FLCs are widely employed for self-justifying DC buses in SSCB systems, thanks to their intuitive, rule-based structure. As illustrated in Figure 7, the Mamdani FLC processes inputs such as current, voltage, and infection using fuzzy rules based on expert knowledge. In operation, the system first fuzzifies these precise inputs into linguistic variables representing conditions like low, normal, or high. The Mamdani inference engine then applies a series of IF-THEN rules to determine the appropriate control response. For example, if the current is high and the voltage is low, the controller may signal the SSCB to separate the course to prevent damage. Finally, the fuzzy output is defuzzified into a crisp control indication, providing adaptive and reliable defense for the DC bus.

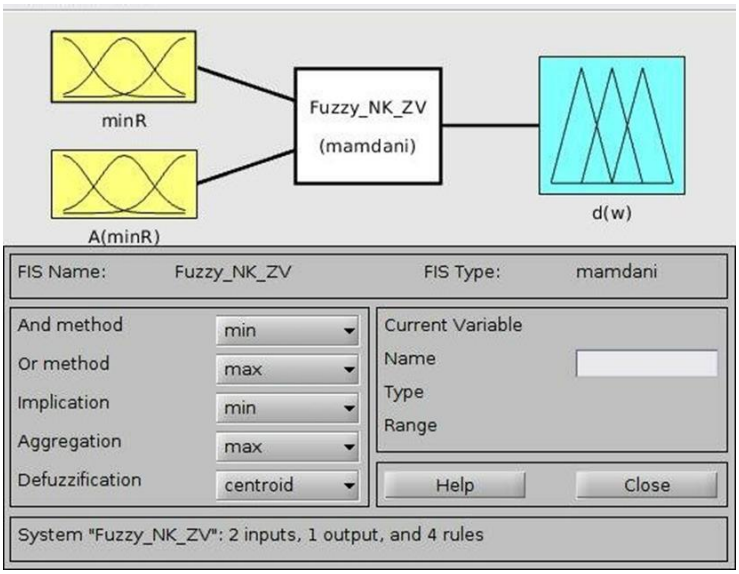


Figure 7. Mamdani type of FLC

5. FLOWCHART OF FUZZY LOGIC CONTROLLER

Figure 8 shows the flowchart of FLC. The flowchart depicts an FLC that adjusts a system's duty ratio (D). The process starts with setting the duty ratio, then measuring the voltage ($V_{in}(k)$) and current ($I_{in}(k)$). These observations are used to compute the power ($P_{in}(k)$). The error (e) is then calculated using the difference in power and voltage between subsequent stages. Changes in error (Δe) are also calculated. These values are fuzzified and then analyzed by an inference engine and a rule base to produce a control signal. This signal is defuzzified in order to alter the duty ratio, which iterates the process.

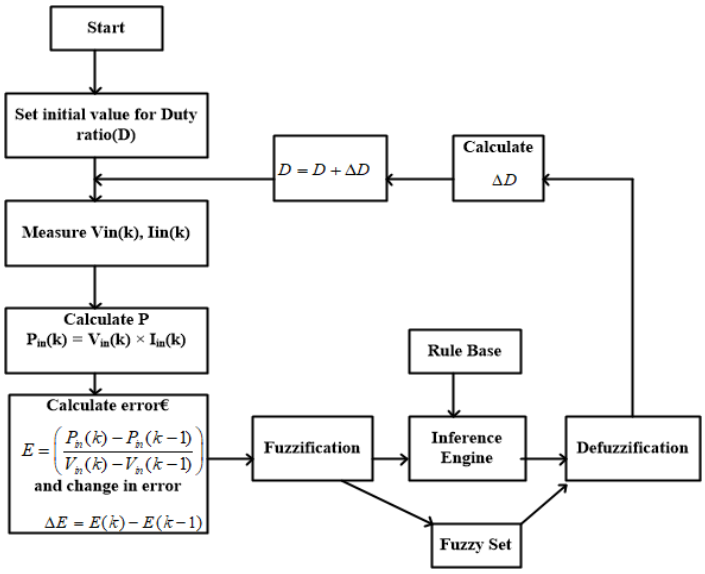
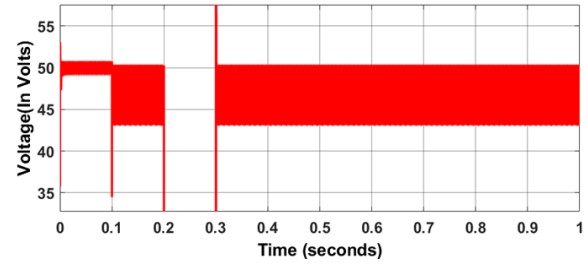


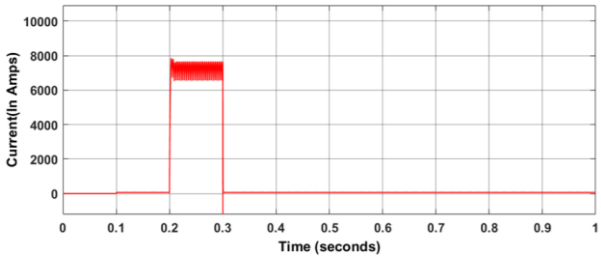
Figure 8. Flowchart of FLC

6. SIMULATION RESULTS

Figure 9 illustrates the normal conduction of the waveforms of the supply voltage (Figure 9(a)) and current (Figure 9(b)). Initially, the supply voltage remains stable at approximately 52 V. However, at around 0.2 seconds, it drops sharply to about 42 V, as seen in Figure 9(a). During a fault event, the voltage briefly spikes before falling completely within 2 milliseconds. Despite the disturbance, distributed energy storage (DES), energy storage components, and connected loads on the DC network remain unaffected. Simultaneously, the source current-starting at 60 amps-surges rapidly to approximately 11,000 amps at 0.2 seconds due to a manually induced fault, and remains at that level for 0.3 seconds, as shown in Figure 9(b). The SSCB responds by clearing the fault within 2 milliseconds, effectively protecting the system components. Following a transport delay of 0.1 seconds, the circuit breaker re-closes the circuit, completing the process in a total of 0.3 seconds. This action restores both the supply voltage and current to their normal operating levels. The results highlight the SSCB's ability to detect and isolate faults far more rapidly than traditional protection systems, ensuring quick recovery, and continued system stability.



(a)



(b)

Figure 9. Normal conduction of (a) the waveform of the supply input voltage and (b) the waveform of the supply input current

Figure 10 shows that under the fault state, one end of the transmission current rises to over 11,000 A under the fault state, as seen in Figure 10(a), whereas the additional end of the main current droplets to zero, as seen in Figure 10(b). The existing differences between the two endpoints are now getting close to 11,000 A. The 'ON' and 'OFF' switches are then turned on by a signal from the AND gate. The line currents at both ends of the DC bus are depicted by the waveforms in Figure 10(c). While IR represents the line current passing through the DC loads, IF represents the responsibility current at the faulty end of the DC bus. The fault transient, or ID, is determined by subtracting IR from IF. FLC-based protection can address the issue in 2 milliseconds.

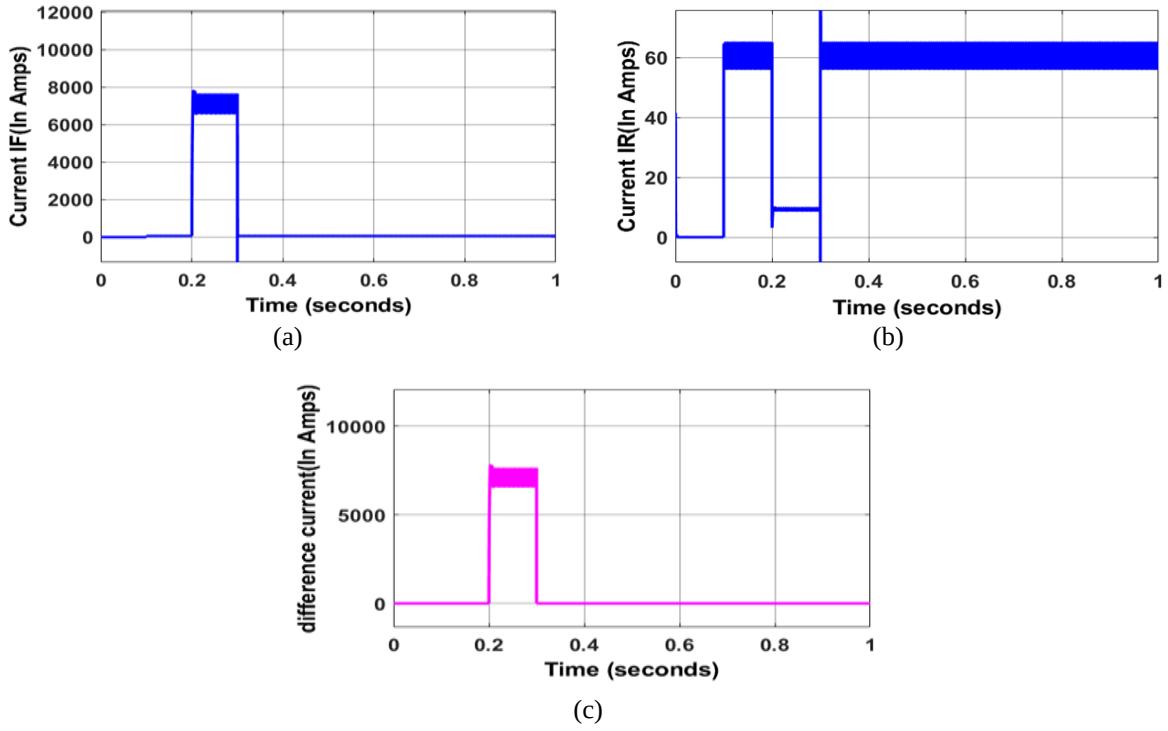


Figure 10. Under the fault state of (a) the fault line current, (b) rated line current, and (c) difference current

Figure 11 shows that under normal operating conditions, the voltage stays constant in Figure 11(a). In contrast, the voltage drops to zero in a failure situation. The current waveform in Figure 11(b) exhibits a similar pattern, beginning at roughly 68 amps and subsequently dropping to about 10 amps at the same time interval until leveling off. The instantaneous variation of the inductance (L) and capacitance (C) load causes the produced voltage to decrease until it hits zero as the no-crossing point increases. When capacitance C is fully charged, the voltage across its inductive load stabilizes and falls to a low value, signifying that the supply and load sides have successfully separated.

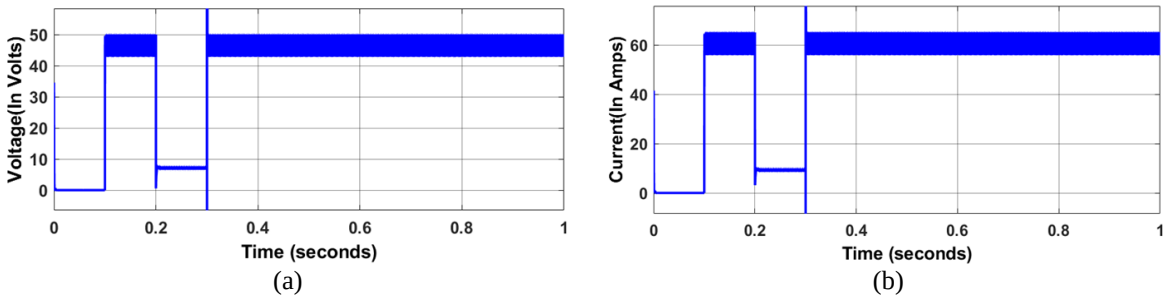
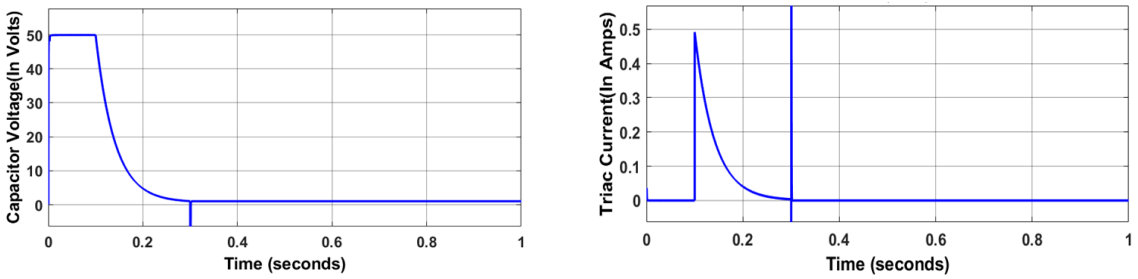


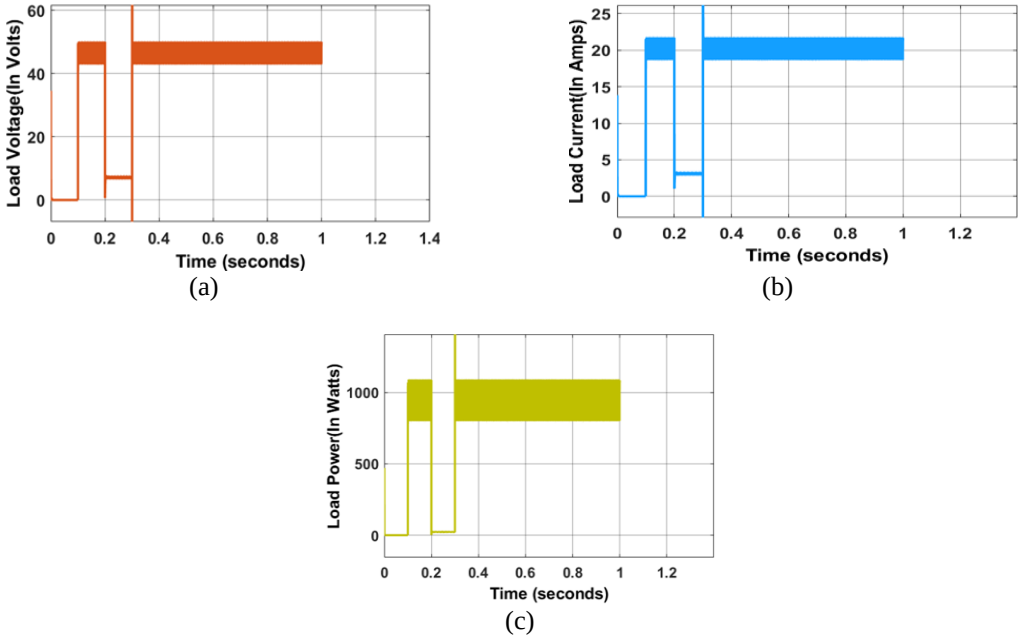
Figure 11. Under normal operating conditions of (a) output voltage and (b) output current

Figure 12 shows the capacitor exhibits distinct charging and discharging behaviors during two key stages: the blocking capacitor accusing stage and the dump umph releasing stage. As shown in Figure 12(a), following a short-circuit fault, the capacitor voltage rapidly increases, reaching a peak of 52 V at around 100 milliseconds. Since the circuit is designed with a reclosing time of 0.3 seconds, the capacitor begins discharging shortly thereafter. Figure 12(b) illustrates this discharging process, where the capacitor voltage drops almost to zero by approximately 0.302 seconds. At the same time, the TRIAC current decreases to zero. During discharge, the peak TRIAC current reaches only 0.1 A, remaining within a safe operating range and having minimal effect on the TRIAC's performance. Figure 13 illustrates the system's behavior through three waveforms. Figures 13(a)-13(c) display the waveforms for load voltage, load current, and load power, respectively, in a system connected to a DC bus. The load remains protected and isolated from the fault current, which occurs between 0.2 seconds and 0.3 seconds, ensuring continued stable operation of the connected devices.



(a) (b)

Figure 12. Charging and discharging of (a) voltage waveform across the capacitor and (b) current waveform through TRIAC



(a) (b) (c)

Figure 13. Illustrates the system's behavior through three waveforms of (a) load voltage, (b) load current, and (c) load power

When comparing the FLC protection method to the traditional differential protection technique, a key advantage becomes evident significantly faster fault response. Although the fault duration is 0.1 seconds in both cases, the fuzzy logic-based protection clears the fault in just 2 milliseconds, whereas the differential protection method requires approximately 4 milliseconds to respond, as shown in Table 2. This faster transient and clearance time highlights the superior efficiency and responsiveness of the FLC approach.

Table 2. Displays the fault-clearing times for differential protection and FLC

Protection strategy	Fault time (seconds)	Fault clearing time (milliseconds)
Differential	0.1	4
Fuzzy logic control	0.1	2

5. CONCLUSION

Compared to the FLC protection method, the traditional differential protection technique exhibits a longer fault transient and clearance time. Although the fault duration remains 0.1 seconds in both scenarios, the FLC resolves the issue within 2 milliseconds, whereas the differential protection method takes approximately 4 milliseconds to clear the fault.

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AUTHOR CONTRIBUTIONS STATEMENT

This journal uses the Contributor Roles Taxonomy (CRediT) to recognize individual author contributions, reduce authorship disputes, and facilitate collaboration.

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Askani Jaya Laxmi		✓			✓	✓		✓		✓		✓		✓

C : **C**onceptualization
M : **M**ethodology
So : **So**ftware
Va : **Va**lidation
Fo : **Fo**rmal analysis
I : **I**nvestigation
R : **R**esources
D : **D**ata Curation
O : Writing - **O**riginal Draft
E : Writing - Review & **E**diting
Vi : **Vi**sualization
Su : **Su**pervision
P : **P**roject administration
Fu : **Fu**nding acquisition

CONFLICT OF INTEREST STATEMENT

The authors declare that they have no conflicts of interest to disclose.

DATA AVAILABILITY

Data availability is not applicable to this paper as no new data were created or analyzed in this study.

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