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Solar photovoltaic based cascaded multilevel inverter with 33-levels using phase opposition disposition control method

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ABSTRACT

A cascaded multilevel inverter (MLI) tailored for photovoltaic (PV) networks, aiming to improve power quality and support transformer-less operation. The symmetric MLI design is selected for its effectiveness in minimizing harmonics and enhancing fault tolerance in high-power scenarios, where the use of power semiconductor converters can introduce complications. The proposed inverter configuration achieves thirty-three voltage levels, optimizing power quality while using insulated gate bipolar transistor (IGBT) semiconductor switches. The phase opposition disposition (POD) control method is applied to trigger necessary switching signals for the inverter's components. To ensure high output voltage for the MLI, a boost converter is employed, and the overall system is tested with an R load. The effectiveness of the design is validated through MATLAB/Simulink simulations, which demonstrate a notable reduction in total harmonic distortion (THD).

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1. INTRODUCTION

The standard inverter has been widely used for years in commercial purposes and low-power systems. However, challenges arise when applied to large power and mid-range power systems, where these specific inverters struggle to meet voltage requirements due to their inability to effectively reduce harmonic content. Conventional inverters tend to have high switching losses, lower efficiency, and shorter lifespans because of long-term stress. This has led to the development of multilevel inverters (MLIs), which generate numerous direct current (DC) levels unified into a sinusoidal waveform, effectively reducing harmonic distortion. Given the increasing global energy demand and the rising cost and limited availability of conventional fuels, solar power has emerged as a promising renewable energy solution. Solar power can be harnessed in DC form using photovoltaic (PV) systems, which can then be converted into grid-quality alternating current (AC) by inverters.

While traditional inverters are still used to gaining popularity in DC to AC conversion due to their capacity to produce a staircase waveform that reduces harmonic distortion, minimizes voltage stress, and boosts power quality [1]. MLIs, particularly the cascaded H-bridge multilevel inverter (CHBMLI) used in distribution static compensators (DSTATCOMs), help reduce source current harmonics and improve power quality. When paired with a proportional-integral (PI) managing device, CHBMLIs can compensate for inductive power, minimize source current harmonics, and maintain unity power factor in distribution systems [2]–[4]. By synthesizing AC voltage from DC, MLIs are rising incrementally common in robust power

grid-bound engineering applications. Specialists have formulated multiple control solutions to increase MLI performance, such as applying active power filters to better power quality and neutralize reactive power. Series active power filters (SAPF) are often used in low and medium-voltage systems to reduce harmonics and compensate for voltage distortions, such as sags, flickers, and notches. SAPF can inject voltage into the line, minimizing total harmonic distortion (THD) and mitigating distortions in the system [5].

As limited energy assets sources like coal, oil, and water deplete, clean energy is transforming into increasingly important. Wind, solar, and hydroelectric power are key players in the push toward clean energy and environmental sustainability. THD is a crucial metric for analyzing the harmonic content of waveforms, and MLIs have shown promising results in reducing voltage THD. Numerous studies on MLIs focus on evaluating voltage THD through numerical analysis and frequency spectra observations. Stepped H-bridge triple-phase converters, for example, are assessed across the time and frequency spectrum to determine the quality assessment of load phase voltage. MLIs are known on behalf of their high-power density and efficiency, making them especially useful in high-voltage-gain applications.

Ultra-lift converters, which offer very high output transfer gains against other voltage increase methods like super-lift and standard boost converters, have been analyzed in continuous conduction mode for their smaller size and improved efficiency [6], [7]. While the quality of voltage regulation has improved with MLIs, this arrives at the cost of increased voltage stress on switches. Each of the three main MLI designs-cascaded, diode-clamped, and flying capacitor-implements its own method for voltage clamping. In diode-clamped MLIs, diodes limit the terminal voltage, while capacitors are used in flying capacitor MLIs. By synthesizing steps from the capacitor voltage, the staircase voltage is formed [8]–[10]. Voltage clamping plays a vital role in generating multilayer output. Clamping devices are used to limit the terminal voltage of a switch within a sufficient range. In diode-clamped MLIs, diodes are responsible for clamping waveforms, while capacitors serve this function in flying capacitor MLIs. In cascaded MLIs, distinct voltage sources are used in the structure. A hybrid harmonic suppression scheme has been proposed to enhance the adaptability of virtual synchronous generators (VSGs), combining the voltage harmonic control loop with the grid current control loop [11]–[13]. MLIs, especially with configurations such as cascaded, diode-clamped, and flying capacitor, play a key role in modern power systems by improving waveform quality, reducing harmonics, and enhancing overall system performance [14], [15]. The THD for assuring the quality of the output voltage measurement is essential. In the proposed MLI system with the phase opposition disposition (POD) control method, the THD can be minimized by incrementing the power level, resulting in the THD content are to be declined. Thus, merit is enhanced as the power level is boosted.

2. PROPOSED PV SYSTEM

The mechanism consists of an electrical load powered via a 33-level MLI, which is moderated using a POD strategy. The MLI receives its direct voltage supply from a boosting converter built to provide peak power tracking control to the PV system, which delivers a regulated DC output voltage. Insulated gate bipolar transistor (IGBT) shifting is employed, and IGBTs are cascaded. This technology offers the benefit of supplying power with higher quality than conventional inverters. Solar cells, compared to other energy sources, are undoubtedly more convenient for standalone applications. The MLI generates thirty-three output electrical voltage levels by utilizing a pulse-width modulation (PWM) technique and specifically the POD control method. Figure 1 represents a clear block diagram of the proposed system.

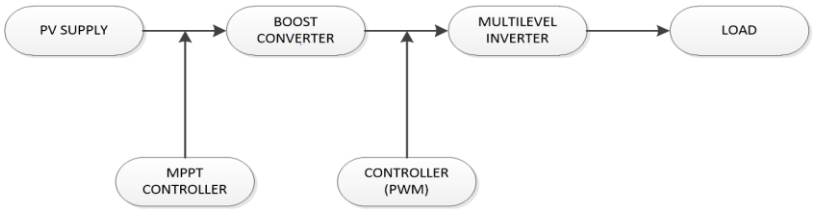

Figure 1. Block diagram of the proposed system

2.1. PV source

In the model of the PV solar cell displayed in Figure 2, the current generated by the solar cell acts as directly proportional to the sunlight intensity received by the cell. However, when the load resistance increases, the PV cell is unable to upload a steady electrical charge output. PV configuration acts as illustrated and connected to a maximum power point tracking (MPPT) managing device to derive the peak

amount of current under varying sunlight conditions. Solar cells are interconnected in series or parallel to achieve the desired voltage and power values. A DC voltage step-up regulator is incorporated to increase the DC output voltage from the PV system as well as ensure peak power extraction [16].

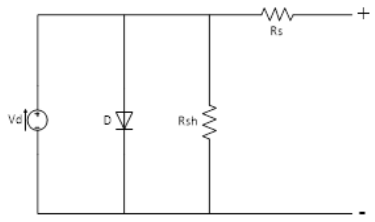

Figure 2. PV model

2.2. Boost converter

Figure 3 represents a clear diagram of a boost converter. A boost converter is employed to elevate the DC input voltage from the PV system. Functioning as a switched-mode power supply (SMPS), the converter consists of a diode and a transistor. At the time the switch is in the "ON" state, the diode is under reverse polarization, isolating the load from the input. During this period, the capacitor distributes energy into the system while the energy is preserved in the inductor. Conversely, when switched "OFF", the diode is polarized in the forward direction, allowing current transferred to flow to the load. During this mode, the input and the energy retained in the inductor deliver power to the load, producing an output voltage higher than the input voltage [17]. The converter operates as part of the perturb and observe (P&O) algorithm to perform MPPT, thus ensuring efficient power regulation and a consistent DC output voltage.

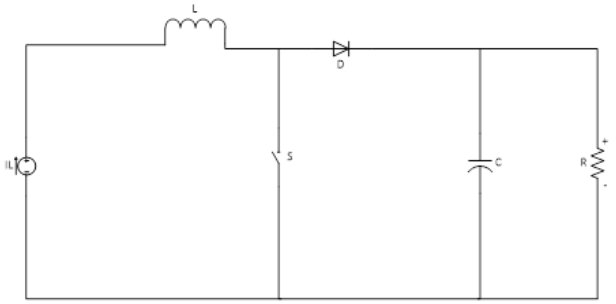

Figure 3. Boost converter

2.3. Multilevel inverter system

A cascaded MLI can be controlled using various methods, with the PWM control technique being most appropriate in this case. In the sine PWM technique, both the modulated signal and carrier signal are used. If only one carrier is present, it is referred to as single-carrier PWM. Multiple carrier PWM command strategies are also applied. The MLI stages are implemented using a cascaded H-bridge (CHB) architecture, which consists of multiple H-bridge inverter cells integrated in order. Each H-bridge cell is powered using a dedicated DC electrical source, which is likely to be sourced from a PV array or a DC-DC converter. The CHB stage generates several voltage levels by switching the H-bridge cells in a coordinated manner [18]. To understand the topology related to an MLI with n levels, (n-1) commutating devices are essential per single phase. To establish an n-level inverter:

$$m = 2n + 1 \quad (1)$$

where m stands for the number of output voltage levels, and n indicates the number of H-bridge cells per phase (each requiring 4 switches). This paper discusses the POD technique. For an m-level inverter, m-1 carrier waves are needed, with half of them shifted by 180°. In the desired control method, as shown in Figure 4, four carrier signals are used-two in the top half are in phase, while the other two in the lower division are 180° out of phase with the uppermost area.

The PV-fed MLI is designed utilizing the POD-PWM technique to enhance voltage stability. It is formed of a PV source, and CHBMLI controls the POD-PWM approach. The voltage (Vpv) generated

originating in the PV system, supplied approaching the CHB-MLI, connected a resistive load (R load). Pulses are formulated using the POD-PWM technique and forwarded to the inverter to achieve the necessary output voltage level [19].

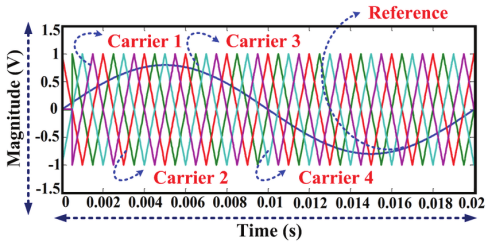

Figure 4. POD-PWM technique

2.4. Multicarrier pulse-width modulation

The most widely adopted governing method for conventional inverters is the sinusoidal PWM technique, in addition referred to as "lower-harmonic" PWM. Its popularity is due to its simplicity and reliability across various operating conditions. This method is easily adaptable for MLIs as well. In the case of an M-level inverter (M-1), triangular modulated waves are attributed to the identical range regularity required [20], [21]. Frequency modulation index (m_f), which is the ratio of carrier frequency to modulating signal frequency, is defined in (2).

$$m_f = \frac{f_{cr}}{f_m} \tag{2}$$

Where f_m is the frequency of the modulating signal and f_{cr} is the frequency of modulating waves. Range modulation index m_a is defined by (3).

$$m_a = \frac{v_m}{v_{cr}(m-1)} \tag{3}$$

Where v_m is the amplitude of the modulating signal and v_{cr} is the amplitude of the carrier waves.

3. SIMULATION RESULTS

The arrangement of the proposed 33-level, 64-switch sequential MLI-associated PV system was successfully deployed using MATLAB/Simulink. By utilizing a boost converter, the system maximizes the power output from the solar source, ensuring that the DC link voltage is adequately maintained. This voltage powers a 33-level MLI, which converts it into a stepped AC voltage. Specifically, the system starts with a 480 V DC input, which is transformed into a 33-level AC output, as shown in Figure 5. Additionally, THD MLI output voltage was monitored, as depicted in Figure 6. The observed THD was 3.41%, which indicates a significant reduction in harmonic distortion. An increasing number of voltage levels directly contributed to the aim of lowering THD, which in turn improved the quality of the output voltage. Figure 6 shows aggregate harmonic distortion in the MLI voltage. Through Figure 6, it is observed that the THD value is 3.41%. Therefore, an increasing number of voltage levels further lowers THD.

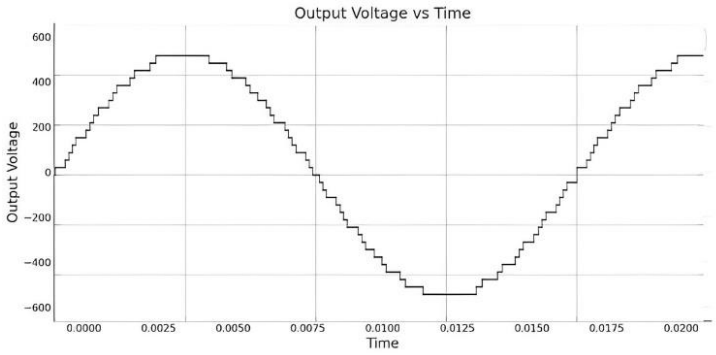

Figure 5. Output of the MLI

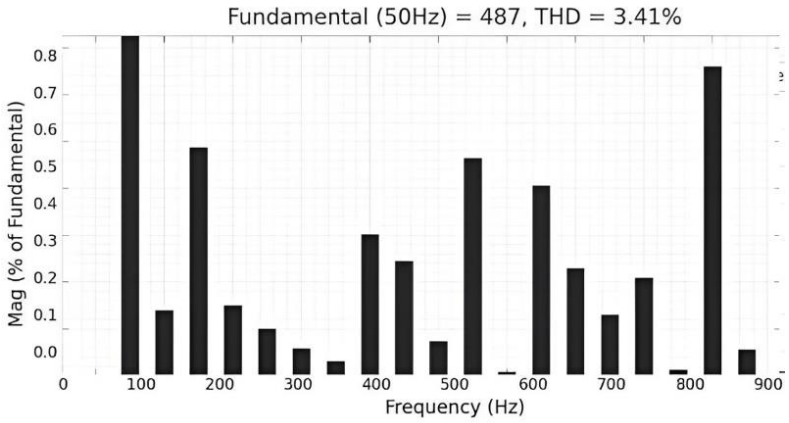

Figure 6. THD of the MLI voltage

4. PERFORMANCE COMPARISON AND DISCUSSION

The performance of the proposed MLI was evaluated against other existing topologies. Table 1 provides a detailed comparison of different inverter topologies and their corresponding THD percentages. For instance, in [22], a 5-level inverter topology resulted in a THD of 37.5%, while in [23], the THD for a 7-level inverter was 16.77%. Similarly, in [24], a 9-level inverter yielded a THD of 14.18%, and in [25], an 11-level inverter recorded a THD of 10.53%. Meanwhile, a 15-level inverter, as shown in [26], produced a THD of 6.18%. In contrast, the proposed 33-level inverter achieved a lower THD of 3.41%, clearly demonstrating that increasing the number of levels contributes to better power quality. As seen in Figure 7, the comparison highlights how the proposed inverter significantly outperforms other topologies, especially in terms of reducing harmonic distortion. Therefore, measuring THD is crucial to ensure the quality pertaining to the output. As voltage levels increase, harmonic interference is found to decrease. Thus, the quality improves with the rise in voltage levels.

Table 1. THD comparison of different inverter topologies

Number of voltage levels	(%) THD output
5-Level inverter [22]	37.5
7-Level inverter [23]	16.77
9-Level inverter [24]	14.18
11-Level inverter [25]	10.53
15-Level inverter [26]	6.18
33-Level inverter (proposed topology)	3.41

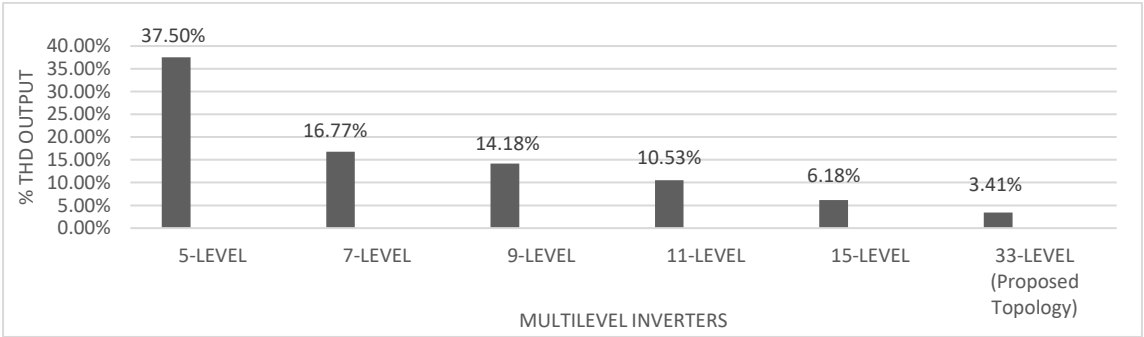

Figure 7. Comparison of different MLIs with THD values

5. CONCLUSION

The present study examines PV-based single-phase cascaded 33-level MLI, where voltage is boosted via a boost power converter to secure high voltage from the DC origin of a sustainable solar facility.

By employing POD, the system's THD is lowered, improving power quality. In this paper, the proposed single-phase 33-level inverter transforms the DC input voltage into a sinusoidal waveform with THD of 3.41%, which is lower than the 6.18% THD obtained from a 15-level CHB-MLI.

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AUTHOR CONTRIBUTIONS STATEMENT

This journal uses the Contributor Roles Taxonomy (CRediT) to recognize individual author contributions, reduce authorship disputes, and facilitate collaboration.

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Madhu Babu Thiruveedula	✓	✓		✓	✓	✓	✓			✓		✓	✓	
Bandari Rahul Teja	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
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Panuganti Yeshwanth Kumar	✓			✓	✓		✓	✓		✓	✓	✓	✓	✓

C : **C**onceptualization
M : **M**ethodology
So : **So**ftware
Va : **Va**lidation
Fo : **Fo**rmal analysis
I : **I**nvestigation
R : **R**esources
D : **D**ata Curation
O : Writing - **O**riginal Draft
E : Writing - Review & **E**diting
Vi : **Vi**sualization
Su : **Su**pervision
P : **P**roject administration
Fu : **Fu**nding acquisition

CONFLICT OF INTEREST STATEMENT

Authors state no conflict of interest.

DATA AVAILABILITY

The data that support the findings of this study are openly available in [2022 International Conference on Communication, Computing and Internet of Things (IC3IoT)] at https://doi.org/10.1109/IC3IOT53935.2022.9767729, reference number [26].

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