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Design of A New Three Phase Hybrid H-bridge and H-Type FCMLI for Various PWM Strategies

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ABSTRACT

The inverters have to be designed to obtain a quality output voltage or a current waveform with a minimum amount of ripple content. In high power and high voltage applications the conventional two level inverters, however, have some limitations in operating at high frequency mainly due to switching losses and constraints of the power device ratings. Series and parallel combination of power switches in order to achieve the power handling voltages and currents. The conventional two level inverters produce THD levels around 60% even under normal operating conditions which are undesirable and cause more losses and other power quality problems too on the AC drives and utilities. Nowadays, multilevel inverters are widely used in power industry. Voltage unbalance problem is one of the major issues in working of multilevel inverter. In this paper, a three phase H-bridge + H-type FCMLI using sinusoidal reference, third harmonic injection reference, 60 degree reference and stepped wave reference are initially developed using SIMULINK and then implemented in real time environment using dSPACE. The five level output voltages of the chosen MLIs obtained using the MATLAB and dSPACE based PWM strategies and the corresponding % THD, V_{RMS} (fundamental), CF and FF are presented and analyzed. It is observed that bipolar COPWM-C provides output with relatively low distortion for sine reference and bipolar COPWM-B strategy is found to perform better since it provides relatively higher fundamental RMS output voltage for 60 degree reference.

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1. INTRODUCTION

In the recent past, the multilevel inverters have drawn tremendous attention in the field of high voltage and high power applications. One of the most important problems in controlling a multilevel voltage source inverter is to obtain a variable amplitude and frequency sinusoidal output by employing simple control techniques. In voltage source inverters, the non fundamental current harmonics cause power losses, electromagnetic interference and pulsating torques in AC motor drives. So the harmonic reduction must be related to performance of an inverter. Multilevel voltage source inverter has various Pulse Width Modulation control schemes have been developed and the same were analyzed in the previous chapter with respect to reduction in power quality issues as discussed by Corzine et al (2003). Multilevel inverter can increase the power by (m-1) times than that of two level inverter through the series and parallel connection of semiconductor power switches. Compared this with two level inverter system delivers same power, the

multilevel inverter has some advantages of that the lower harmonic components on the output AC voltages can be eliminated and EMI problem could be decreased. Babaei et al., (2014) the topology requires lesser number of power switches and dc voltage sources. Banaei et al. (2014) the proposed inverter works with lower total peak inverse voltage. Kangarlu et al., (2013) the multilevel inverter uses reduced number of power switching devices. Special focus has been paid to obtain optimal structures regarding different criteria such as number of dc voltage sources, standing voltage on the switches, number of switches. Odeh et al., (2013) analysis of the conduction power losses in the power semiconductor switches of the proposed inverter topology. Chung-Ming Young et al., (2013) the combination of batteries can be controlled according to the batteries voltages to implement the battery-balancing function. Panda et al., (2012) cascaded multilevel inverter with low-frequency three-phase transformers and a single dc power source is proposed. This topology aims to reduce the number of components and so reduce the complexity of the circuit. Zixin et al. (2012) the level of the output voltage is only half of the dc-link voltage in all conditions, leading to much reduced dv/dt. Yi-Hung et al., (2011) the studied multistring inverter topology offers strong advantages such as improved output waveforms, lower electromagnetic interference and THD. Hinago et al., (2010) the proposed inverter can output more numbers of voltage levels in the same number of switching devices by using this conversion. The number of driving circuits is reduced, which leads to the reduction of the power consumption and size in the driving circuits. The THD value of the output waveform is also reduced. Naumanem et al., (2010) pulsed inverter voltage and the impedance mismatch between the cable and the motor cause an oscillating overvoltage in the motor terminals.

2. H-BRIDGE AND H-TYPE FCMLI

Figure 1 shows the different types of multilevel inverters. In this work, a H-bridge will produce three output levels and H-type FCMLI will produce five output levels. Both the modules are connected in series. So the total output is $V_{dc1} + V_{dc2} = V_o$. The output voltage across the load will have seven levels and the number of carriers required to produce seven output levels is six carriers. Multi-carrier bipolar triangular carrier modulation strategies with different references are employed for the study of the chosen MLI. Figure 2 shows the power circuit for three phase H-bridge and H-type FCMLI. The multilevel inverters are classified as follows:

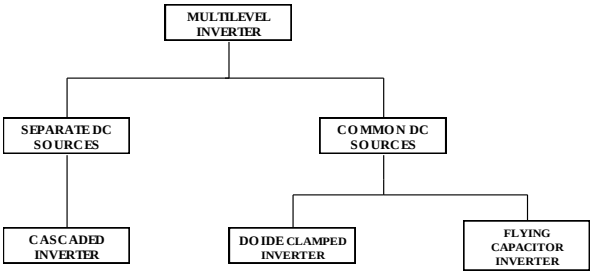

Figure 1. Types of multilevel Inverters

Table 1 displays the switch states and output voltage levels for H-bridge and H-type flying capacitor multilevel inverter.

Table 1. H-bridge and H-type flying capacitor multilevel inverter - switch states and output voltage levels

H-type FCMLI								H-Bridge				V_{ao}	V_{bo}	V_{ab}
S_{a1}	S_{a2}	S_{a3}	S_{a4}	S_{b1}	S_{b2}	S_{b3}	S_{b4}	S_{a1}	S_{a2}	S_{b1}	S_{b2}			
0	0	1	1	1	1	0	0	1	0	0	1	-Vdc	Vdc	-2Vdc
0	0	1	1	1	1	0	0	0	1	0	1	-1/2 Vdc	1/2Vdc	-Vdc
0	0	1	1	0	1	0	1	0	1	0	1	-1/2 Vdc	0	-1/2 Vdc
0	1	0	1	1	1	0	0	0	1	0	1	0	1/2 Vdc	-1/2 Vdc
1	0	1	0	1	1	0	0	0	1	0	1	0	-1/2 Vdc	1/2 Vdc
1	1	0	0	1	1	0	0	0	1	0	1	1/2 Vdc	1/2 Vdc	0
0	0	1	1	0	0	1	1	0	1	0	1	-1/2 Vdc	-1/2 Vdc	0
0	1	0	1	0	0	1	1	0	1	0	1	0	-1/2 Vdc	-1/2 Vdc
1	1	0	0	0	1	0	1	0	1	0	1	1/2 Vdc	0	1/2 Vdc
1	0	1	0	0	0	1	1	0	1	0	1	0	-1/2 Vdc	1/2 Vdc
1	1	0	0	0	0	1	1	0	1	0	1	1/2 Vdc	-1/2 Vdc	Vdc
1	1	0	0	0	0	1	1	0	1	1	0	Vdc	-Vdc	2Vdc

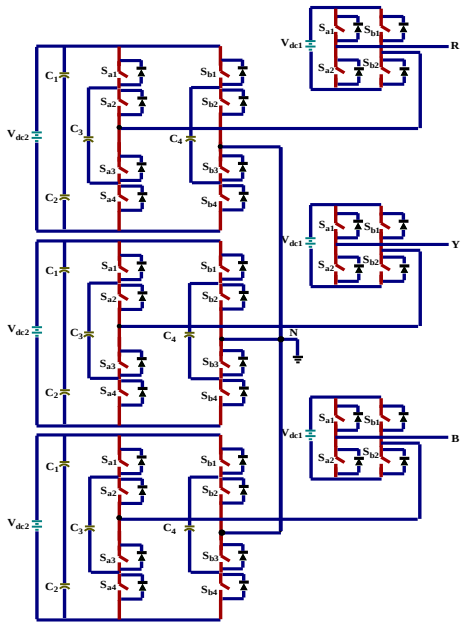

Figure 2. Three phase H-bridge and H-type flying capacitor multilevel inverter

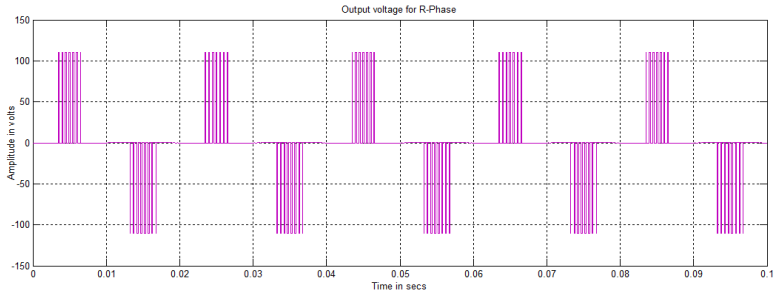

Figure 3. Output voltage of H-bridge for R-Phase

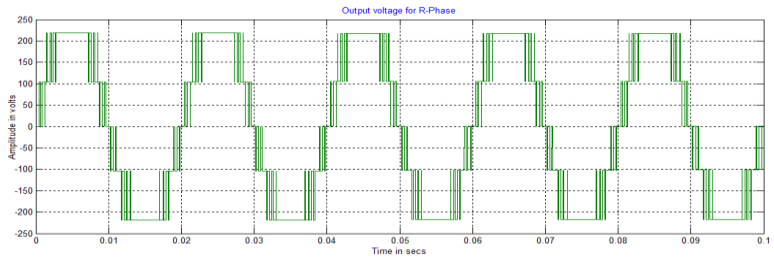

Figure 4. Output voltage of H-type FCMLI for R-Phase

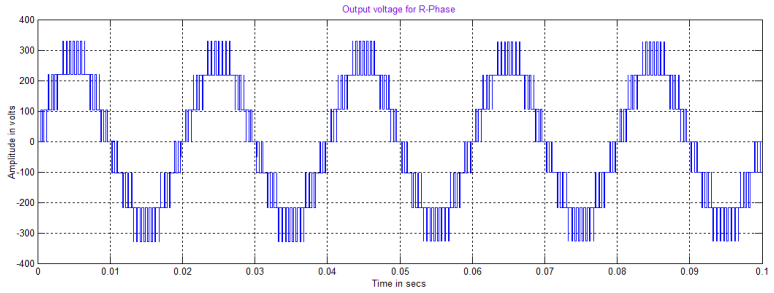

Figure 5. Total Output voltage of H-bridge + H-type FCMLI for R-Phase

3. PWM STRATEGIES

High-switching-frequency modulation methods like multicarrier bipolar PWM and space vector modulation techniques have been used for MLI modulation control. The proposed topology can be modulated with any one of these methods with suitable adjustment. In the present work, the multicarrier bipolar PWM scheme is used. Figure 6 and 7 shows the sample carrier arrangement. In a multicarrier bipolar PWM scheme, carrier signals are compared with the reference signal, and the pulses obtained are used for switching of devices corresponding to respective voltage levels. In the proposed topology, one switch may contribute for synthesis of more than one level at output terminals.

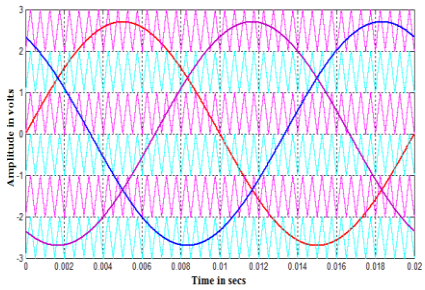

Figure 6. Sample carrier arrangement for sinusoidal reference and PDPWM strategy

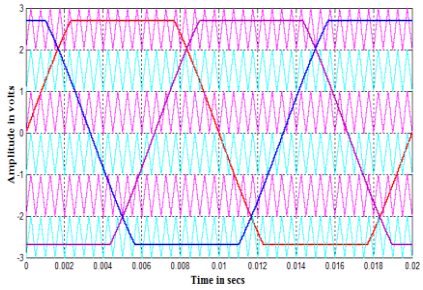

Figure 7. Sample carrier arrangement for 60 degree reference and PDPWM strategy

4. SIMULATION RESULTS

The simulated output voltage is shown for only one sample value of m_a=0.8. The following parameter values are used for simulation: V_{dc1} = 110V, V_{dc2} = 440V, R(load) = 100 ohms, C_1 = C_2 = 10 e-3 Farad and C_3 = 1600 Farad, f_c =2000 Hz and f_m = 50 Hz. Figure 8, 10, 12 and 14 shows the sample output voltage for PDPWM strategy with sinusoidal, THI, 60 degree and stepped wave reference and the corresponding FFT plot is shown in Figure 9, 11, 13 and 15. Table 2-5 show the comparison of %THD, V_{RMS} (fundamental), CF and FF for different PWM strategies with various references.

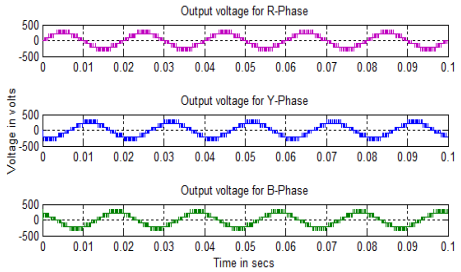

Figure 8. Sample output voltage generated by PDPWM strategy for H-bridge and H-type FCMLI with sine reference

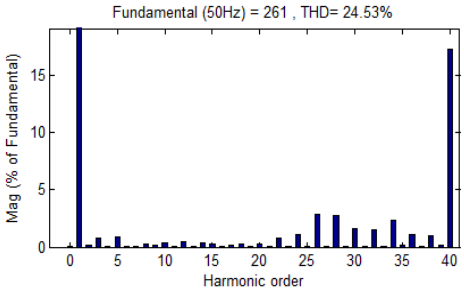

Figure 9. FFT plot for output voltage generated by PDPWM strategy for H-bridge and H-type FCMLI with sine reference

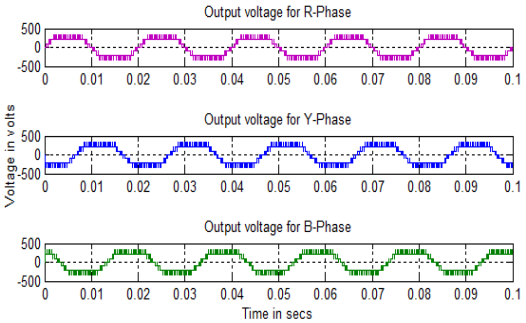

Figure 10. Sample output voltage generated by PDPWM strategy for H-bridge and H-type FCMLI with THI reference

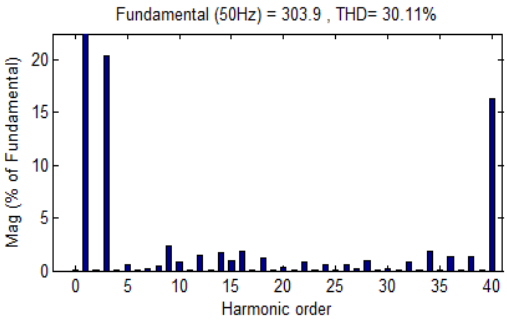

Figure 11. FFT plot for output voltage generated by PDPWM strategy for H-bridge and H-type FCMLI with THI reference

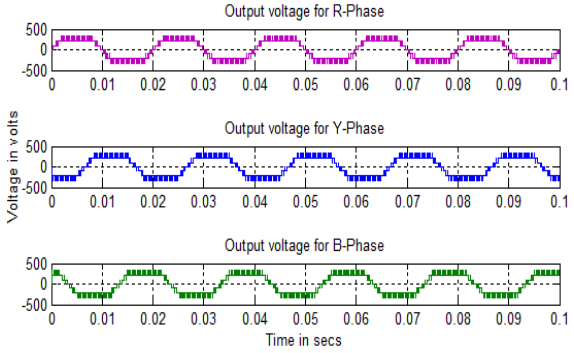

Figure 12. Sample output voltage generated by PDPWM strategy for H-bridge and H-type FCMLI with 60 degree reference

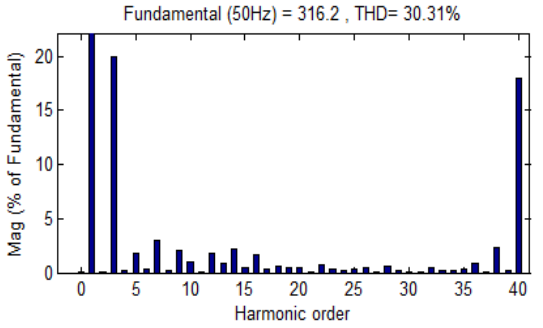

Figure 13. FFT plot for output voltage generated by PDPWM strategy for H-bridge and H-type FCMLI with 60 degree reference

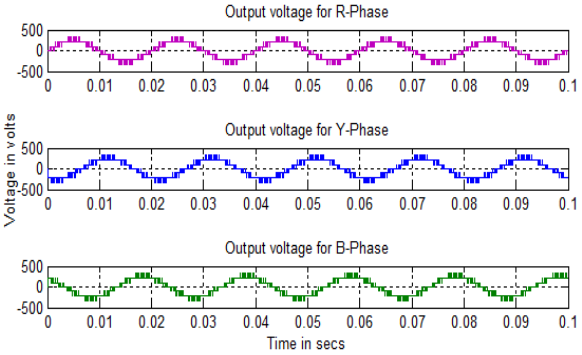

Figure 14. Sample output voltage generated by PDPWM strategy for H-bridge and H-type FCMLI with stepped wave reference

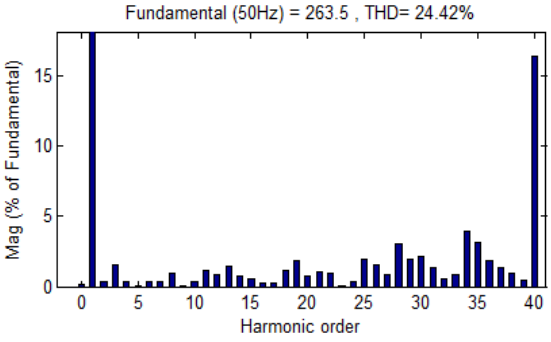

Figure 15. FFT plot for output voltage generated by PDPWM strategy for H-bridge and H-type FCMLI with stepped wave reference

Table 2. % THD of output voltage (R-phase) of H- bridge and H-type FCMLI for various values of m_a (R-load, by simulation)

m_a	Sinusoidal reference							Third harmonic injection reference						
	PD	POD	APOD	CO-A	CO-B	CO-C	VF	PD	POD	APOD	CO-A	CO-B	CO-C	VF
1	18.35	18.28	18.11	22.81	21.26	16.85	18.41	24.97	25.06	24.92	28.22	28.04	26.37	24.98
0.9	22.58	22.29	22.86	26.37	24.05	18.78	22.63	29.12	29.03	29.68	30.93	29.29	27.32	29.17
0.8	24.53	24.32	24.39	29.38	27.83	21.90	24.56	30.11	29.92	30.92	32.84	31.46	29.47	30.16
0.7	25.86	25.48	25.62	33.55	32.23	23.65	25.83	27.80	27.65	28.09	34.49	33.50	29.39	27.86
0.6	34.75	34.66	34.06	40.98	40.68	25.21	34.62	36.66	36.14	35.72	41.86	42.28	29.28	36.71
m_a	60 degree PWM reference							Stepped wave reference						
	PD	POD	APOD	CO-A	CO-B	CO-C	VF	PD	POD	APOD	CO-A	CO-B	CO-C	VF
1	22.69	22.49	22.59	26.88	28.10	26.47	22.72	16.78	16.87	17.12	22.39	22.64	17.84	16.77
0.9	28.17	28.08	28.53	29.98	28.10	26.13	28.23	23.14	23.05	22.82	26.13	24.44	19.01	23.08
0.8	30.31	29.94	31.26	32.44	30.94	29.16	30.39	24.42	24.69	23.92	29.10	27.70	20.48	24.41
0.7	27.78	28.04	28.06	33.65	31.93	29.02	27.84	27.26	27.28	25.99	33.30	32.81	24.43	27.24
0.6	34.05	33.79	33.53	40.62	40.47	29.98	34.06	34.52	35.27	32.91	40.98	40.41	27.04	34.53

Table 3. V_{RMS} of output voltage (R-phase) of H- bridge and H-type FCMLI for various values of m_a (R-load, by simulation)

m_a	Sinusoidal reference							Third harmonic injection reference						
	PD	POD	APOD	CO-A	CO-B	CO-C	VF	PD	POD	APOD	CO-A	CO-B	CO-C	VF
1	231.8	231.5	232.6	247.1	255.5	255.2	231.8	268.7	269.5	268.8	276.6	283.3	282.9	268.7
0.9	208.6	209.1	208.6	230.4	241.1	241	208.5	241.8	241.8	242.1	258.7	270.5	270.4	241.7
0.8	184.5	184.5	185.6	212.4	222.6	222.3	184.6	214.9	214.8	215.5	240.8	252.8	252.7	214.8
0.7	161	160.4	162.5	191.1	201.4	200.1	161	187.5	187.6	188.2	320.8	232.9	232.7	187.6
0.6	136.7	136.7	138.8	164.2	173.1	172.1	136.7	159.6	159.7	161.4	189.1	199.9	199.4	159.6

m_a	60 degree PWM reference							Stepped wave reference						
	PD	POD	APOD	CO-A	CO-B	CO-C	VF	PD	POD	APOD	CO-A	CO-B	CO-C	VF
1	279.8	280.1	280	283.4	285.5	285	279.8	233.4	234	234.7	248.7	255.7	255.6	233.4
0.9	251.6	251.8	252	265.8	277.4	277	251.6	209.8	210.1	212.5	230.5	242.7	240.7	209.8
0.8	223.6	223.4	223.9	246.4	257.4	257.5	223.6	186.3	186.2	189.3	213.4	223.8	220.9	186.3
0.7	195.3	195.8	195.7	226.3	240.6	240.3	195.3	162	162.1	165.1	191.3	203.3	200.2	162
0.6	166.3	166.1	167.6	197.1	208.1	207.4	166.3	137.3	136.8	140.1	165.8	173.2	171	137.2

Table 4. CF of output voltage (R-phase) of H- bridge and H-type FCMLI for various values of m_a (R-load, by simulation)

m_a	Sinusoidal reference							Third harmonic injection reference						
	PD	POD	APOD	CO-A	CO-B	CO-C	VF	PD	POD	APOD	CO-A	CO-B	CO-C	VF
1	1.4141	1.4141	1.4140	1.4140	1.4144	1.4141	1.4141	1.4142	1.4144	1.4140	1.4143	1.4140	1.4142	1.4145
0.9	1.4137	1.4139	1.4146	1.4144	1.4143	1.4141	1.4139	1.4139	1.4143	1.4142	1.4139	1.4144	1.4145	1.4145
0.8	1.4146	1.4138	1.4137	1.4143	1.4141	1.4143	1.4138	1.4141	1.4143	1.4143	1.4140	1.4141	1.4143	1.4143
0.7	1.4136	1.4142	1.4141	1.4139	1.4131	1.4142	1.4142	1.4144	1.4147	1.4144	1.4142	1.4139	1.4129	1.4141
0.6	1.4147	1.4140	1.4135	1.4142	1.4142	1.4137	1.4140	1.4141	1.4139	1.4138	1.4145	1.4142	1.4132	1.4141
m_a	60 degree PWM reference							Stepped wave reference						
	PD	POD	APOD	CO-A	CO-B	CO-C	VF	PD	POD	APOD	CO-A	CO-B	CO-C	VF
1	1.4138	1.4141	1.4142	1.4142	1.4140	1.4143	1.4142	1.4143	1.4145	1.4141	1.4145	1.4141	1.4143	1.4143
0.9	1.4145	1.4142	1.4142	1.4142	1.4142	1.4144	1.4145	1.4142	1.4140	1.4141	1.4143	1.4140	1.4137	1.4142
0.8	1.4141	1.4140	1.4152	1.4139	1.4141	1.4139	1.4141	1.4143	1.4146	1.4141	1.4142	1.4137	1.4142	1.4143
0.7	1.4142	1.4141	1.4144	1.4144	1.4143	1.4140	1.4147	1.4141	1.4145	1.4136	1.4140	1.4146	1.4140	1.4135
0.6	1.4143	1.4136	1.4146	1.4145	1.4142	1.4136	1.4137	1.4136	1.4144	1.4139	1.4143	1.4139	1.4146	1.4139

Table 5. FF of output voltage (R-phase) of H- bridge and H-type FCMLI for various values of m_a (R-load, by simulation)

m_a	Sinusoidal reference							Third harmonic injection reference						
	PD	POD	APOD	CO-A	CO-B	CO-C	VF	PD	POD	APOD	CO-A	CO-B	CO-C	VF
1	1363.5	3311.4	7753.3	4118.3	12775	12760	3311.42	746.38	26950	26880	747.56	28330	28290	767.71
0.9	1604.6	1603.8	5215	1645.7	12055	12050	1603.84	1209	12090	12105	3695.7	27050	27040	24170
0.8	3890	1678.1	3712	21240	7420	7410	1678.18	7163.3	10740	10775	24080	25280	25270	7160
0.7	847.36	670.83	2031.2	1124.1	5035	5002.5	670.83	3125	6253.3	6273.3	32080	11645	11635	1443.0
0.6	3417.5	3417.5	1067.6	1642	2472.82	2458.57	3417.5	840	2281.4	2305.7	6303.3	49975	4985	INF
m_a	60 degree PWM reference							Stepped wave reference						
	PD	POD	APOD	CO-A	CO-B	CO-C	VF	PD	POD	APOD	CO-A	CO-B	CO-C	VF
1	2543.6	28010	28000	944.66	28550	28500	2798	9336	7800	234.7	3108.7	12785	12780	416.78
0.9	12580	25180	25200	984.44	27740	27700	6290	999.04	5252.5	212.5	794.82	12135	8023.3	428.16
0.8	2795	11170	11195	24640	25740	25750	1490.66	1552.5	2315.7	189.3	646.66	7460	7363.3	503.51
0.7	1395	6526.6	6523.3	2514.4	12030	12015	781.2	5400	1140	165.1	1125.2	5082.5	5005	540
0.6	475.14	2768.3	2793.3	19710	6936.66	6913.3	1847.77	624.09	3724	140.1	1658	2886.6	2442.8	4573.3

5. CONCLUSION

In this paper, a three phase new hybrid topology of H-bridge + H-type FCMLI using sinusoidal reference, third harmonic injection reference, 60 degree reference and stepped wave reference are initially developed using SIMULINK. The five level output voltages of the chosen MLIs obtained using the MATLAB based PWM strategies and the corresponding % THD, V_{RMS} (fundamental), CF and FF are presented and analyzed. From tables it is observed that bipolar COPWM-C provides output with relatively low distortion for sine reference and bipolar COPWM-B strategy is found to perform better since it provides relatively higher fundamental RMS output voltage for 60 degree reference.

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