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Novel Design of Reversible MUX and DEMUX using GDI Techinque

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ABSTRACT

Now a day's Reversible logic is playing a crucial role in designing of digital circuits and it is used in reducing power consumption in digital design. By regaining the bit loss it reduces the power consumption in digital circuits. Gate diffusion input (GDI) is a technique of low-power digital circuit design. This technique reduces the power consumption, delay, and transistor count by maintaining the complexity very low of logic design. In these paper a novel MUX and DEMUX has been presented, which can be extended up to 1:2n and 2n:1 respectively and these are developed by using only one type of Reversible gate i.e. Fredkin Gate (FRG) and Not Gate. The simulations are done in H-Spice using 90nm technology.

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1. INTRODUCTION

Today's advancement in level of integration and fabrication process has getting better logic circuits and energy loss has also been dramatically reduced. According to Landauer principle [1], in every logic computation a bit of information loss generates kTln2 joules of heat energy where k is the Boltzmann constant of 1.38×10^{-23} J/K and T is the absolute temperature of the environment. Reversible circuits are basically different from traditional irreversible ones. In reversible logic, no information is lost. Bennett [2] showed that zero energy dissipation would be possible if the network consists of reversible gates only. But the drawback is area will be increased compared to irreversible circuits even though Reversible Gates are much better than conventional CMOS [3].

A reversible circuit should have the following attributes [4]:

1. Garbage output should be as minimum as possible.
2. Number of reversible gate should be as minimum as possible.
3. Input lines that are either 0 or 1, known as constant input, should be as minimum as possible.

There are different types of styles logical design like,

Pass Transistor Logic (PTL): There are two basic problems [5] one is threshold drop across pass transistor results in slower operations of circuits and other problem is that there will be direct static path for power dissipation due to PMOS device in the inverter circuit is not fully turned off.

Transmission gate (TG): It solves the low logic level swing problem by using PMOS and NMOS Connected Complementary Pass-transistor Logic (CPL): The CPL suffers from static power consumption due to the low swing at the gates of the output inverters [6].

Gate Diffusion Technique (GDI) is a low power technique which solves the most of problems mentioned above. The GDI approach allows implementation of a wide range of complex logic functions

using only two transistors. This method is suitable for design of fast, low-power circuits, using a reduced number of transistors (as compared to CMOS and existing PTL techniques), while improving logic level swing and static power characteristics and allowing simple top-down design by using small cell library.

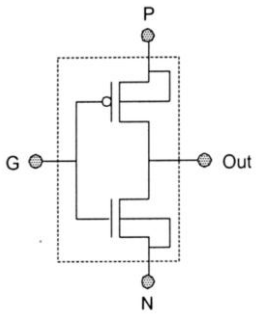

Figure 1. GDI basic cell

The GDI method is based on the use of a simple cell as shown in Figure 1. At first look, the circuit reminds one of the standard CMOS inverter, but there are some important differences.

1) The GDI cell contains three inputs: G -common to gate input of nMOS and pMOS, P -input to the source/drain of pMOS, and N -input to the source/drain of nMOS [7].

2) Bulks of both nMOS and pMOS are connected to N or P (respectively), [7].

MUX and DEMUX are the basic building blocks of so many digital circuits or digital logics. But reversible designs of MUX and DEMUX are more complex than the conventional MUX and DEMUX, since there are equal no .of inputs and outputs; fan-out of a signal is only one, feed-back is not allowed in the reversible logic; and the primary inputs are needed to be restored at the output [8]. Here we show reversible realizations of 2:1, 4:1 MUX and 1:2, 4:1 DEMUX. MUX plays an important role in FPGA functionalities. So to design a MUX with reversible logic using GDI technique will create a new idea of designing low power FPFA circuits.

2. BACK GROUND AND BASIC CONCEPTS

Basic Gates like AND Gate, OR Gate, XOR Gate designed by using GDI is very useful in designing Reversible Gates. The major design issue in GDI is we have to choose always a proper W/L Ratios and VDD otherwise the output will distorted sometimes output will be wrong due to improper choosing of W/L Ratio.

2.1. AND GATE

The design of AND Gate using CMOS requires 6 transistors but using GDI it requires 2 transistors only [9].

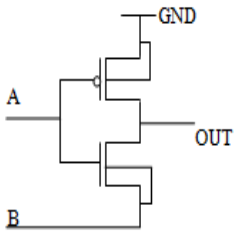

Figure 2. AND Gate

2.2. OR GATE

The design of OR Gate using CMOS requires 6 transistors but using GDI it requires 2 transistors only [9].

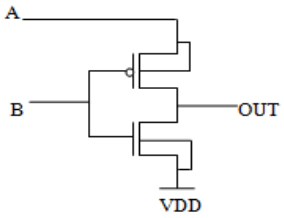

Figure 3. OR Gate

2.3. XOR GATE

The design of XOR Gate using CMOS requires 12 transistors but using GDI it requires 4 transistors only [9].

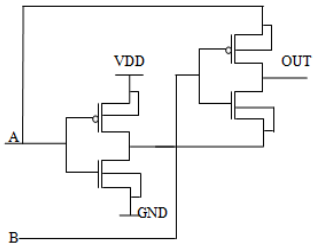

Figure 4. XOR Gate

3. PROPOSED REVERSIBLE GATE USING GDI

Proposed Reversible gate is Fredkin Gate (FRG). This gate is designed by GDI structure so that there will be a reduction in large amount of power, transistor count and delay.

3.1. FREDKIN GATE

It is also called Controlled Swap Gate (CSWAPG). It is a universal 3*3 gate, which means that any logical or arithmetic operation can be constructed totally by Fredkin gate. The Fredkin Gate is the three bit gate that swaps the last two bits if first bit is 1 [4].

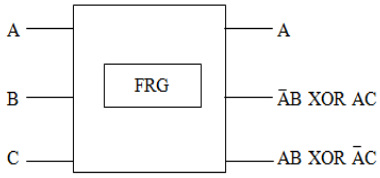

Figure 5. FREDKIN GATE

4. PROPOSED REVERSIBLE MUX USING GDI TECHNIQUE

A MUX is a device that performs multiplexing operation; it selects one digital input signals by using select signal and forwards the selected input into a single line. The FRG gate is used for the designing the multiplexers [10]. Figure 6 and Figure 7 shows the 2:1 and 4:1 multiplexer design respectively using proposed logic and special feature in this design is that, it has enable signal, by using this signal we can control the MUX like on and off whenever we want. So by using the enable signal we can use this MUX as switch.

When,

1. ENABLE [E] = 0; Output will be Zero means MUX is in OFF state.
2. ENABLE [E] = 1; Output will be One means MUX is in ON state.

Table 1. 2:1 MUX Truth Table

Enable Signal (E)	Input	Select Signal (S)	Output
0	D0	0	Y0 =0
1	D0	0	Y0 =D0
1	D1	1	Y0 =D1

When,

1. Select signal [S] is Zero, Data1 line-D0 is selected and forwarded to output.
2. Select signal [S] is One, Data2 line-D1 is selected and forwarded to output.

The above truth table says that there is no change in the functionality of 2:1 reversible multiplexer using GDI with respect to the irreversible conventional CMOS multiplexer functionality. The equation for the output Y is given as follows:

Output with enable signal is Y0=ED0S' + ED1S

The Proposed Reversible MUX using GDI technique has been implemented by Fredkin Gate as shown as below.

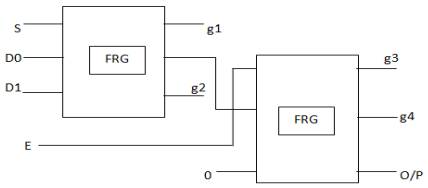

Figure 6. Block diagram for 2:1 Reversible MUX using GDI Technique

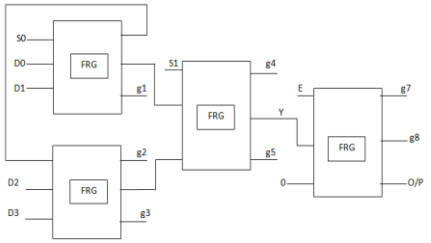

Figure 7. Block diagram for 4:1 Reversible MUX using GDI Technique

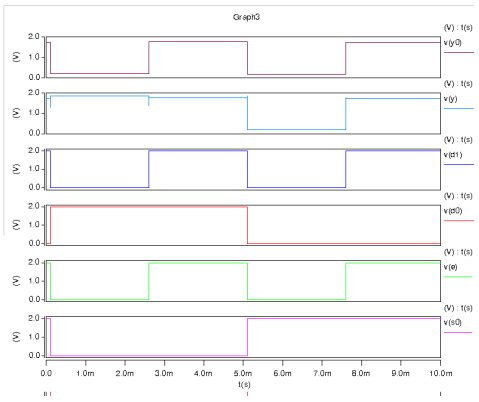

Figure 8. Simulated waveform of proposed 2:1 MUX

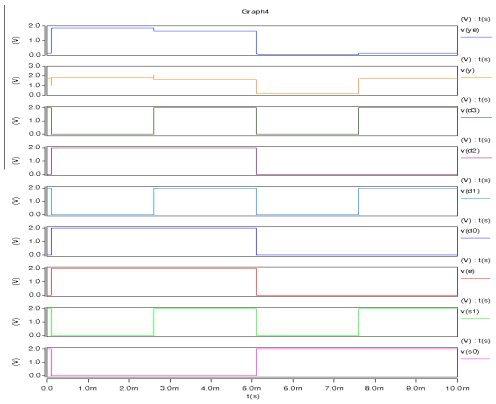

Figure 9. Simulated waveform of proposed 4:1 MUX

Table 2. Comparision of Table 1

Logical Style	MUX	Power	Transistor Count	Garbage Outputs
GDI	2:1	0.1 mW	36	4
	4:1	0.2 mW	72	8

The major advantages of this design is,

1. By using this enable signal in MUX, we can make the circuit to go into the sleep mode.
2. Outputs Glitch strength will get reduce by using the enable signal
3. Less no. of garbage outputs will be produced by using this design compared to [9].

5. PROPOSED REVERSIBLE DEMUX USING GDI TECHNIQUE

DEMUX are sometimes more convenient for designing general purpose logical designs, because if the DEMUX's input is always correct or true, the DEMUX acts as a decoder. The selection bits function can be constructed by simple logically OR-ing of the correct set of o/p's [10].

A DEMUX is a device taking a single input signal and select one of many data output- lines, which is connected to the single input. A MUX is mostly used with a complementary DEMUX at the receiving end.

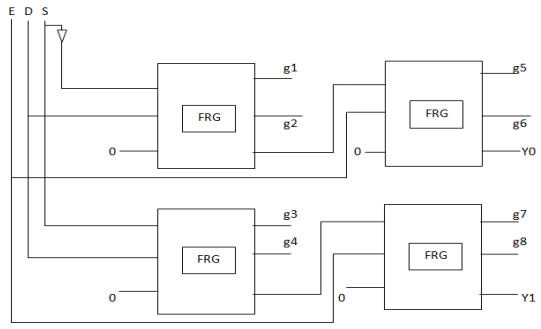

Figure 10. Block diagram for 2:1 Reversible DEMUX using GDI Technique

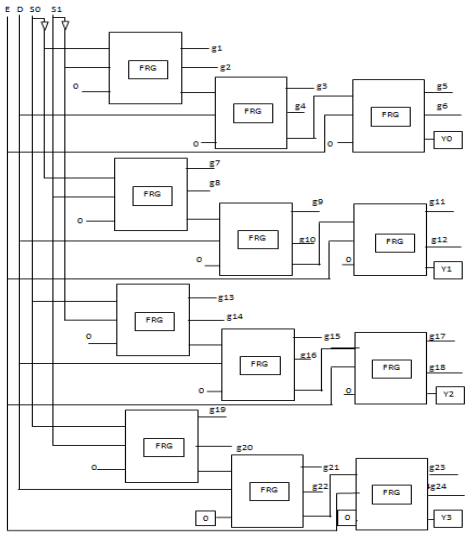

Figure 11. Block diagram for 4:1 Reversible DEMUX using GDI Technique

When,

1. ENABLE [E] = 0; O/P will be Zero means DEMUX is in OFF state\
2. ENABLE [E] = 1; O/P will be One means DEMUX is in ON state

So, we use enable signal like a switch for DEMUX.

Table 3. 1:2 DEMUX Truth Table

Enable Signal (E)	Input	Select Signal (S)	Output
0	D	0	0
1	D	0	Y0 =D
1	D	1	Y1 =D

When,

1. Select signal [S] is Zero, output y0 is selected and data is forwarded to output.
2. Select signal [S] is One, output y1 is selected and data is forwarded to output.

The above truth table says that there is no change in the functionality of 1:2 reversible DEMUX using GDI technique with respect to the irreversible conventional CMOS DEMUX functionality. The equation for the output Y is given as follows:

Output1 with enable, when S =0; Y0=EDS'

Output2 with enable, when S =1; Y1=EDS

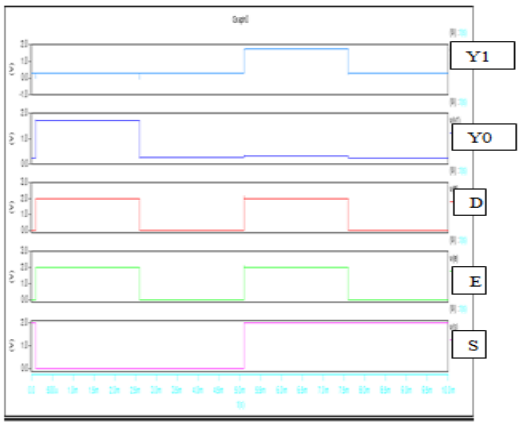

Figure 12. Simulated waveform of proposed 2:1 DEMUX

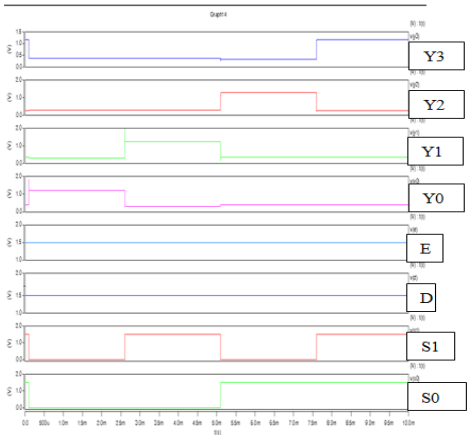

Figure 13. Simulated waveform of proposed 4:1 DEMUX

The major advantages of this design is:

1. By using this enable signal in DEMUX, we can make the circuit to go into the sleep mode.
2. The design is simple because if we use other than Fredkin Gate then transistor count and garbage values will get increases.
3. Outputs Glitch strength will get reduce by using the enable signal
4. Transistor count of the circuit is very less compared to Conventional CMOS.
5. Less no. of garbage outputs will be produced by using this design compared to [9].

Table 4. Comparision of Table 2

Logical Style	DEMUX	Power	Transistor Count	Garbage Outputs
GDI	1:2	0.64 mW	74	8
	1:4	0.9 mW	220	24

6. CONCLUSION

The proposed MUX and DEMUX using GDI technique can be easily extended to 2^n:1 and 1:2^n respectively and it has been implemented by using only one reversible gate i.e. Fredkin Gate and power analysis has been presented in comparison table I and II. The additional and unique feature of this proposed reversible MUX and DEMUX i.e. enable signal, so we can enable or disable the MUX and DEMUX whenever it is required. The simulations are done in H-Spice using 90nm technology file. By using this proposed design the transistor count reduction has been reduced drastically compared to conventional CMOS and garbage values also got reduced by using this proposed design. Major disadvantage of this design is when the circuit design is going for higher bits then the design complexity will increased slightly. Because of GDI Technique definitely there will be power reduction in this proposed design compared to conventional CMOS design.

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