

Effect of Novel Nanocomposite Materials for Enhancing Performance of Thin Film Transistor TFT Model

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ABSTRACT

The potential impact of high permittivity gate dielectrics on thin film transistors short channel and circuit performance has been studied using highly accurate analytical models. In addition, the gate-to-channel capacitance and parasitic fringe capacitances have been extracted. The suggested model in this paper has been increased the surface potential and decreased the threshold voltage, whenever the conventional silicon dioxide gate dielectric is replaced by high-K gate dielectric novel nanocomposite PVP/La₂O₃K_{ox}=25. Also, it has been investigated that a decrease in parasitic outer fringe capacitance and gate-to-channel capacitance, whenever the conventional silicon nitride is replaced by low-K gate sidewall spacer dielectric novel nanocomposite PTFE/SiO₂K_{sp}=2.9. Finally, it has been demonstrated that using low-K gate sidewalls with high-K gate insulators can be decreased the gate fringing field and threshold voltage. In addition, fabrication of nanocomposites from polymers and nano-oxide particles found to have potential candidates for using it in a wide range of applications in low cost due to low process temperature of these nanocomposites materials.

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1. INTRODUCTION

Integrated Circuits IC's can include as many as hundred million transistors or more. As increased gate leakage is one major limiting factor on aggressive scaling effective gate-dielectric thickness will require alternative materials with higher permittivity's K_{ox} and greater physical thicknesses, a factor of (K_{ox}/KSiO₂) to prevent direct gate tunneling [1], [3]. However, the use of a high-K gate material may result in dielectric thicknesses comparable to the device gate length, fringing fields from the gate to the source/drain regions compromising the short-channel performance increasing. Kumar and Chaudhry [4] have earlier developed a model for the threshold voltage for dual material gate SOI-MOSFETs. Our suggested model for the threshold voltage for the single nanocomposite material gate SOI-MOSFETs by including the effect of the internal fringe capacitance on the threshold voltage, which can be easily, solved using a few iterations. In order to accurately characterize TFT devices, the threshold voltage must be well formulated. Our suggested model with novel nano composite material PVP/La₂O₃ with high dielectric constant enhances the performance of MOSFETs. By increasing in the surface potential and decreasing the threshold voltage. It has been demonstrated a suitable low-permittivity low-K gate sidewall spacer dielectric novel nanocomposite PTFE/SiO₂, K_{sp}=2.9, which can replace Si₃N₄, K_{sp}=7.5 [4-11].

The energy of the band edge is the threshold condition for conduction in the TDT (some authors redefine the TDT model as the mobility edge model [12] by modifying the tail shape). It can be shown that

the expressions for μ_0 derive in the TDT [13] and VRH [14] theories differ by two constant multipliers [15]. This setting violates the conditions for proper use of the infinite integration limit in the gamma function in the theoretical derivations in [13], [14]. This problem was recently identified in [16]. The variety of models for OTFTs is large, ranging from simple phenomenological models based on similarities to crystal FETs, to finite-element models of the TFT structure [17], and from the adaptation of a-TFT charge sheet models [18] to limiting models [19]. Each of these models has advantages and disadvantages, addressing different issues such as complexity, accuracy, repeatability, physics, characterization techniques, or convergence. On the other hand, the object of the models is the same accurate prediction of the electrical characteristics of OTFTs. Recently, the fringing capacitance was present through the conformal mapping of potential space. Fringing Induced Barrier Lowering FIBL is the effect of charges induced by the fringing capacitances, a threshold voltage case including the fringing capacitance effect is studied and the influence of gate dielectric on threshold voltage is discussed [20-27].

2. THIN FILM TRANSISTOR TFT MODEL

A model cross-sectional of an SOI-MOSFET with a high-Kok gate dielectric is shown in Figure 1(a), with the fringing field lines from the bottom of the gate electrode to the drain and source regions. For simplicity, that circular field lines as shown in Figure 1(b), and to the approach used in studies for the other components of parasitic capacitance [7], [8]. The infinitesimal capacitances in the high-Kok and spacer regions, respectively can be written as:

$$dC_1 = \frac{K_{ox}Wdy}{\left(\frac{\pi}{2}\right)y}, \text{ and } dC_2 = \frac{K_{sp}Wdy}{\left(\frac{\pi}{2}\right)(t_{ox}-y)} \quad (1)$$

Where K_{ok} is the permittivity of the gate dielectric, K_{sp} is the permittivity of spacer material, W is the width of the transistor structure, and t_{ok} is the gate-dielectric thickness. Since dC_1 and dC_2 are in series, the net infinitesimal capacitance can be written as:

$$dC = \frac{dC_1 dC_2}{dC_1 + dC_2} = \frac{2K_{ox}K_{sp}Wdy}{\pi(K_{ox}t_{ox} + K_{sp}y - K_{ox}y)} \quad (2)$$

The total internal fringe capacitance can be obtained by integrating (2) over the gate-dielectric thickness as fringing:

$$C_{bottom} = \int_0^{t_{ox}} \frac{2K_{ox}K_{sp}Wdy}{\pi(K_{ox}t_{ox} + K_{sp}y - K_{ox}y)} \quad (3)$$

$$C_{bottom} = \frac{2K_{ox}K_{sp}W}{\pi(K_{ox} - K_{sp})} \ln \left(\frac{K_{ox}}{K_{sp}} \right) \quad (4)$$

From the entire perimeter of the bottom edge of the gate electrode as:

$$C = \frac{(2 - \ln 4)K_{ox}}{2\pi} \quad (4)$$

For $K_{ox} = K_{sp}$, and $\frac{t_{ox}}{L_g} \ll 1$

Where: L_g is the gate length.

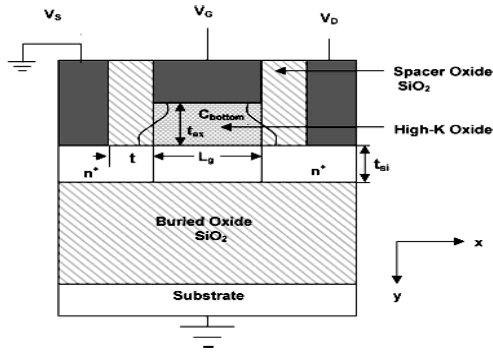


Figure 1(a). Cross-sectional of an SOI-MOSFET, Internal parasitic fringe capacitance

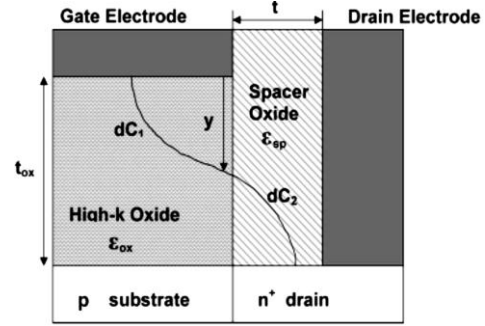


Figure 1(b). Cross-sectional of an SOI-MOSFET, Fringing field bottom of the gate electrode

The total fringe capacitance can be obtained by Equation (4), and the perimeter of the bottom edge of the gate electrode [2]. Since the account for electric field lines fringing from the bottom edge of the gate to either the source or the drain region only, the internal fringe capacitance can be written as:

$$C_{bottom} = \frac{((2-\ln 4)K_{ox}W)}{2\pi} \cong \frac{(0.3)K_{ox}W}{\pi}, \quad (5)$$

For $K_{ox} = K_{sp}$, and $\frac{t_{ox}}{L_g} \ll 1$

It can be seen that Equ. (3) reduces to Equation (5) in the limit $K_{ok} \rightarrow K_{SP}$ but for a constant factor. This difference arises because of the assumption of the fringing electric field lines is being circular while deriving Equation (3). thus, multiplied by the above factor equally 0.15 to obtain:

$$C_{bottom} = \frac{(0.3)K_{ox} K_{sp} W}{\pi(K_{ox} - K_{sp})} \ln \left(\frac{K_{ox}}{K_{sp}} \right) \quad (6)$$

These expression reduces to Equ. (5) the limit $K_{ok} \rightarrow K_{SP}$, and hence Equ. (6), that the separation between the electrodes is very small in comparison to the length of the electrodes [10]. This is certainly not the case in short channel high-k dielectric SOI-MOSFETs. Further modified to represent the true picture, and the fringing field from the gate to the source/drain regions increases as a function of (t_{ox}/L_g) . This is the effect of the increased crowding of field lines in the spacer region for large gate-dielectric thicknesses, for t_{ox} comparable to L_g , the fringe capacitance in the spacer region is more than what has been assumed while Equ. (6). to account for this, an effective spacer dielectric constant as:

$$K'_{sp} = \left(1 + \frac{t_{ox}}{L_g} \right) K_{sp} \quad (7)$$

Substituting (7) in place of K_{SP} in (6), then obtain the final expression for the parasitic internal fringe capacitance as:

$$C_{bottom} = \frac{(0.3)k_{eff}W}{\pi} \quad (8)$$

Where: $k_{eff} = \frac{K_{ox}K'_{sp}}{K_{ox}-K'_{sp}} \ln \left(\frac{K_{ox}}{K'_{sp}} \right)$

2.1. Suggested High-K Gate Dielectric Model and Selected Nano-Materials

The parasitic capacitances are becoming an important issue for designing logic circuits to reduce MOS transistor dimensions into the deep sub-micrometer regime. Hence, an accurate suggested model in of bottom fringing capacitances is necessary to predict circuit performance before fabrication, thus; the suggested model is an efficient tool in designing and characterization of high-K gate-dielectric SOI-MOSFETs including the effects of parasitic internal fringe capacitance [28]. The conventional gate dielectric structure diagram of the TFT devices under study is shown in Figure 2(a), silicon dioxide with dielectric constant $K_{ox}=3.9$ has been used as a gate oxide material for decades. The suggested model structure as shown in Figure 2(b) which includes gate dielectric with high-K value for enhancing the performance TFT devices by using novel nanocomposite with high dielectric constant value $K_{ox}=25$.

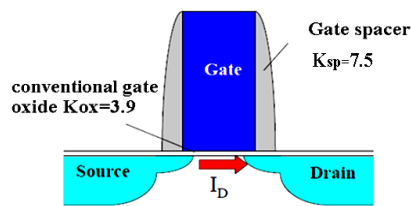


Figure 2(a). Single layer conventional gate dielectric and suggested of gate dielectric TFTs, Conventional gate dielectric oxide

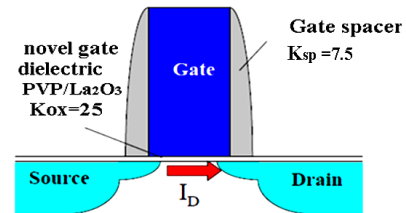


Figure 2(b). Single layer conventional gate dielectric and suggested of gate dielectric TFTs, Novel nanocomposite gate dielectric

The suggested nanocomposite materials have potential candidates for using in a wide range of applications in low cost due to low process temperature of these devices may pave way for achieving high performance for TFT devices. Inserting nanocomposite materials between the gate and S/D contacts are very effective in relaxing the requirements on the virtual source velocity. Lanthanum oxide La_2O_3 blended with polyvinyl phenol PVP instead of silicon dioxide. So that, homogeneous organic-inorganic slurry has been obtained, 10wt% PVP and La_2O_3 nano particles, to introduce a gate dielectric nanocomposite gate with high-k dielectric constant and used in the suggested model. According to the mobility degradation is one of the major challenges for MOSFETs with high-K gate dielectrics, this model MOSFETs with PVP/ La_2O_3 dielectric film has been solved this problem, as PVP which has been enhanced electron mobility and on-off ratios.

2.2. Suggested Low-K Gate Sidewall Spacer Model and Selected Nano-Materials

Estimation of electronic circuit performance is necessary in the design phase to be ensured proper reliability. Thus, fringing capacitance is one of the major contributors to the degradation performance and signal integrity problems in sub-100-nm circuits. Hence, an accurate suggested model of fringing capacitances has been investigated to enhance and predict the circuit performance before fabrication. The conventional gate structure diagram of the TFT devices under study is shown in Figure 3(a) in this structure. Shrinking the conventional MOSFET beyond the 45nm technology node requires innovations to suppress parasitic fringing capacitances and short channel effects. Thus, the suggested model structure as shown in Figure 3(b) has been included gate sidewall spacer value enhances the gate control of short-channel effects SCEs.

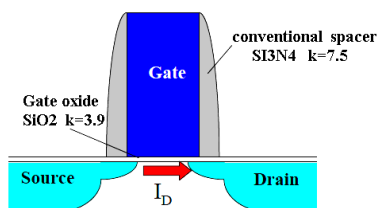


Figure 3(a). A single layer conventional and suggested model of gate spacer TFTs, Conventional gate dielectric spacer

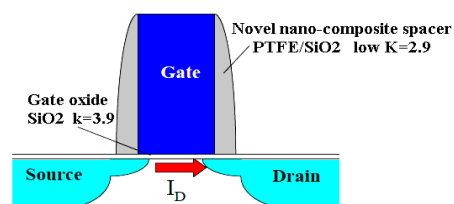


Figure 3(b). A single layer conventional and suggested model of gate spacer TFTs, Novel nanocomposite gate dielectric spacer

Also, reduces the source-to-drain leakage current and enhances the performance TFTs devices by using spacer with low K value $K_{SP}=2.9$ of Silicon dioxide blended with Poly (tetrafluoroethylene) PTFE instead of silicon nitride in the sidewall spacers. Therefore, inserting nanocomposite materials (20wt% SiO_2 nano- particles and PTFE) between the gate and S/D contacts is effective in relaxing the requirements on the virtual source velocity and for introducing a gate dielectric spacer with low-K dielectric constant. If silicon dioxide concentration increases up to value of 20wt%, it may be result in the higher leakage current also structure defects induced by the present of high concentration SiO_2 .

2.3. Estimation of Fringing-Capacitance and Surface Potential of Low-K Gate Sidewall Spacer

From studies cases of MOSFETS [6-16], the fringing capacitances of a low-K gate dielectric are shown in Figure 4, where C_{of} is the gate dielectric fringing capacitance, C_{gf} is the gate electrode fringing capacitance, C_{ox} is the gate dielectric capacitance between the gate and channel, T_{ox} and T_g are the physical thickness of the gate dielectric and gate electrode, respectively, L and L_a are channel length and distance between source/drain electrode and gate dielectric respectively, t is width of overlap region between source/drain and gate electrode, O is the origin of the (x,y) coordinate system.

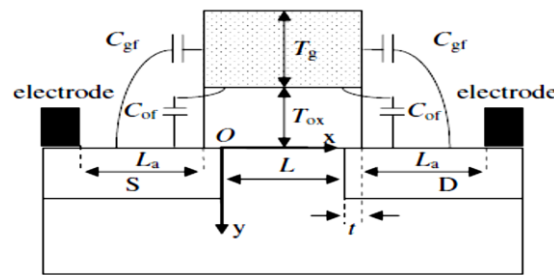


Figure 4. Fringing capacitances for MOSFET

2.4. Estimation of Surface Potential

The field lines terminate at the surface of the source/drain regions, leading to an increase of the gate electrode fringing-capacitance. For a given gate dielectric constant, the gate dielectric fringing-capacitance increases with the dielectric constant of the sidewall spacer. It has been that degradation in short-channel performance with high-k dielectrics is caused by the fringing fields from, because the fringing fields can affect the electric potential in the channel, by weakening the gate control [2]. When V_{ds} is small, $V_d \cong V_s = V_{bi}$. Where V_s and V_d are the source and drain voltages, V_{bi} is built-in potential of the source/substrate and drain/substrate junctions, V_{ds} is the potential difference between drain and source. Thus, the induced charge density at the surface of source or drain region by the fringing field lines of C_{of} is

$$\sigma_{of} = C_{of} \frac{(V_G - V_{bi})}{W L_a} \quad (9)$$

Where $V_G = V_g - V_{fb}$

These charges produce an electric field in the channel, and the relevant surface potential is [7].

$$\Phi(x, 0) = \frac{\sigma_{of}}{8\pi\epsilon_0\epsilon_{si}} \left((x + L_a) \ln(\Phi_1) - x \ln(\Phi_1) + W \ln(\Phi_2) \right) \quad (10)$$

For the same reason, the surface potential induced by C_{gf} can be found:

$$\phi_{gf}(x, 0) = \frac{\sigma_{gf}}{8\pi\epsilon_0\epsilon_{si}} \left((x + L_a) \ln(\Phi_1) - x(\Phi_1) + W \ln(\Phi_2) \right) \quad (11)$$

Where:

$$\Phi_1 = \frac{\sqrt{(x+L_a)^2 + \frac{W^2}{4}} + \frac{W}{2}}{\sqrt{(x+L_a)^2 + \frac{W^2}{4}} - \frac{W}{2}}$$

$$\Phi_2 = \frac{\sqrt{x^2 + \frac{W^2}{4}} + L_a + \sqrt{x^2 + L_a^2 + 2L_a \sqrt{x^2 + \frac{W^2}{4}}}}{\sqrt{x^2 + \frac{W^2}{4}} + x}$$

$$\sigma_{gf} = C_{gf} (VG - V_{bi}).$$

The electric potential of short channel MOSFET without the influence of the fringing fields was derived to be [11]:

$$\phi_s(x, y) = \phi_0(y) + (V_{bi} + V_{ds}) \frac{\sinh(\frac{x}{l})}{\sinh(\frac{L}{l})} + V_{bi} \frac{\sinh(\frac{L-x}{l})}{\sinh(\frac{L}{l})} \quad (12)$$

$$\text{Where } \phi_0(y) \text{ is the electric potential of long channel CMOS; } l = \sqrt{\frac{K_{si} y_d}{C_{ox}}} \quad (13)$$

CMOS; l is a characteristic length describing the short-channel effect; y_d is width of the depletion region in the substrate [11]. Considering the influence of the fringing capacitances, the threshold voltage V_{th} is defined as the gate voltage when the total surface potential at the location of minimum surface potential (x_0)

$$\phi_s(x_0) + \phi_{of}(x_0) + \phi_{gf}(x_0) = 2\phi_B \quad (14)$$

Where: $\phi_B = \frac{k_B T}{q} \ln\left(\frac{N_A}{n_i}\right)$ is the Fermi potential of the substrate, when V_{ds} is small, $x_0 \approx L/2$. Therefore, the threshold voltage can be found by Eqs. (12) and (14)

$$V_{th} = V_{th0} - \frac{2(V_{bi} - 2\phi_B + \phi_{of}(x_0) + \phi_{gf}(x_0))}{2 \cosh(\frac{L}{2l}) - 2} \quad (15)$$

Where, V_{th0} represents the threshold voltage of long channel MOSFET, and the threshold voltage roll-off increases with K_{sp} in the short-channel region.

3. RESULTS AND DISCUSSION

This paper has been discussed the following items: enhancing TFTs using high-K gate dielectric nanocomposite material, enhancing TFTs using low-K gate spacer nanocomposite material, and finally the modification of enhancing TFTs using high-K and low-K gate sidewall spacer with nanocomposite material.

3.1. Enhancing TFTs using High-K Gate Dielectric Nanocomposite Material

Figure 5 and 6 illustrate the effect of nanocomposite gate dielectric film in internal fringe capacitance C_{bottom} by the proposed model. Figure 5 shows the internal fringe capacitance C_{bottom} versus the gate spacer dielectric permittivity. It's cleared that fringing capacitance C_{bottom} increases with inserting K_{ox} by

a novel nanocomposite material higher than conventional gate dielectric. Figure 6 shows the internal fringing capacitance as a function of normalized gate length for a novel and conventional gate dielectrics. This figure illustrates the fringing capacitance C_{bottom} decreases with increasing the gate length from 10nm to 80nm, but PVP/La₂O₃ gives the highest fringing capacitance from conventional gate dielectric with SiO₂, at given drain bias $V_D=0.05$ V.

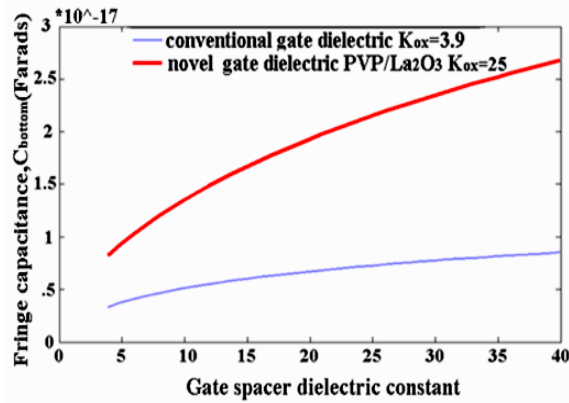


Figure 5. Effect of gate spacer dielectric constant on internal fringing-capacitance C_{bottom} using PVP/La₂O₃ and SiO₂ gate dielectric K_{ox}

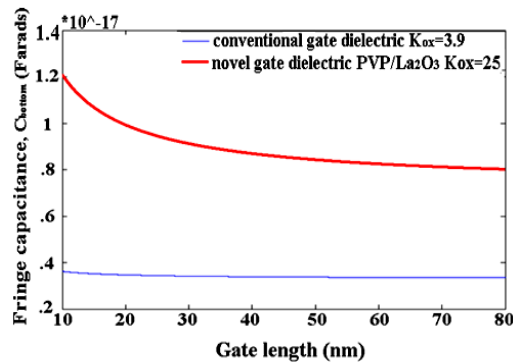


Figure 6 Effect of gate length on internal fringing-capacitance C_{bottom} using PVP/La₂O₃ and SiO₂ gate dielectric K_{ox}

Figure 7 and 8 show the effect of nanocomposite high-K gate dielectric film, and parasitic internal fringe capacitance on the surface potential. Figure 7 shows the influence of high-K dielectrics and sidewall spacers on gate surface potential, it's noticed that novel nanocomposite gate dielectric gives higher surface potential than conventional gate dielectric constant with increasing gate spacer dielectric constant. Fig. 8 shows the calculated surface potential variation along the channel for $K_{\text{ox}}=25$ with and without the effect of the fringe capacitance. Figure 10 shows the effect of nanocomposite gate dielectric film on the threshold voltage. The novel nanocomposite material of PVP/La₂O₃ has low threshold voltage as compared to those with conventional SiO₂ of the same width. Related to high of permittivity of nanocomposite materials, the fringing gate capacitances C_{bottom} much high in TFT devices and so, high permittivity of nano composite material increases the surface potential as a result of the induced charges in the drain and source regions due to fringing field lines from the bottom of the gate electrode. Figure 9 explains that the novel nano composite material PVP/La₂O₃ has less threshold voltage as compared with conventional SiO₂ of the same width. As a result of high permittivity of nanocomposite materials, the fringing gate capacitances C_{bottom} have much high in TFT devices. So, high permittivity of nanocomposite material increases the surface potential of the induced charges in the drain and source regions due to fringing field lines from the bottom of the gate electrode. The drop in the threshold voltage is as high as about 25mV for $L_g=60$ nm as ϵ_{ox} increases from 3.9 to 25. All these results are early onset of inversion the channel and hence lower threshold voltage.

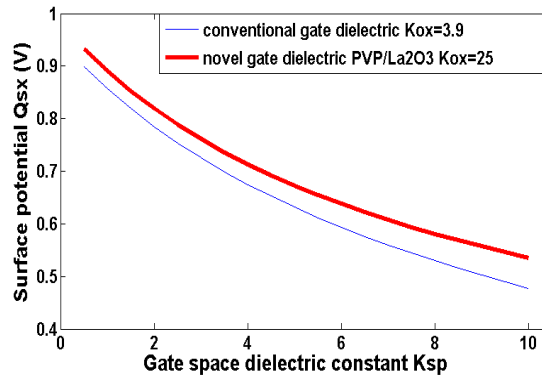


Figure 7. Effect of gate spacer dielectric of nanocomposite high-K gate dielectric film, and parasitic internal fringing capacitance on the surface potential for devices with SiO_2 and high K_{ox} PVP/ La_2O_3 gate dielectric material.

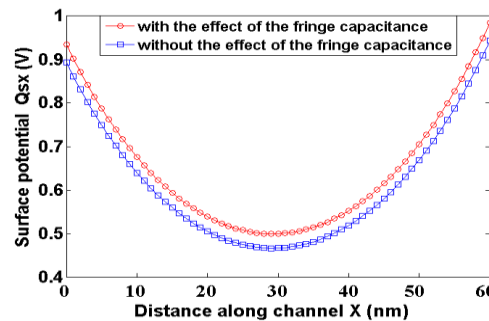


Figure 8. Effect of distance along channel of nanocomposite high-K gate dielectric film, and parasitic internal fringing capacitance on the surface potential for devices with SiO_2 and high K_{ox} PVP/ La_2O_3 gate dielectric material.

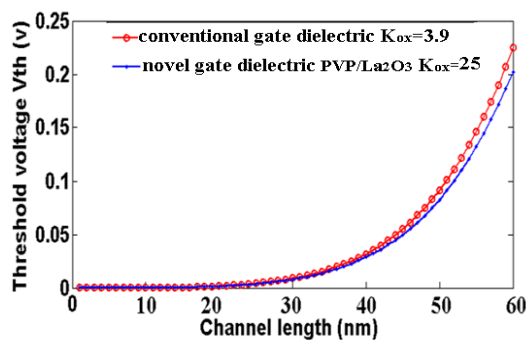


Figure 9. Influence of K_{ox} value of gate dielectric film on the threshold voltage of TFT

3.2. Enhancing TFTs using Low-K Gate Spacer Nanocomposite Material

Figure 10 and 11 illustrate that the effect of nanocomposite sidewall spacer dielectric film gate in electrode fringing capacitance C_{gf} . The suggested model indicates that the electrode fringing capacitance C_{gf} decreases with increasing T_{ox} due to increasing distance between the two plates of C_{gf} . It is cleared that, the calculated results of the electrode fringing capacitance C_{gf} for novel suggested nanocomposite material of side-wall spacer dielectric film gate PTFE/ SiO_2 has lower than the conventional side-wall spacer dielectric film gate Si_3N_4 spacer K_{sp} as shown in Figure 10. In case of Fig. 11, the variation of the gate electrode fringing- capacitance has been shown with varying gate thickness. For a given EOT and K_{ox} , the gate electrode fringing-capacitance increases with T_{g} . Also, it is cleared that, the calculated results of the electrode fringing capacitance C_{gf} for novel suggested nanocomposite material of side-wall spacer dielectric film gate

PTFE/SiO₂ has lower than the conventional side-wall spacer dielectric film gate Si₃N₄ spacer K_{sp} in shown in Figure 11. In case of Figure 12, the effect of nanocomposite sidewall spacer dielectric film has been shown on the gate dielectric fringing-capacitance C_{of}. It is notices that the gate dielectric fringing-capacitance C_{of} by using novel nanocomposite suggested material PTFE/SiO₂ is lower than the gate dielectric fringing-capacitance C_{of} with conventional Si₃N₄, this means that the field lines from the bottom of the gate electrode can easily go through the interface between the gate dielectric and sidewall spacer. Figure 13 shows the threshold voltage roll-off (V_{roll-off} = V_{th} - V_{th0}) for different K_{sp} values of sidewall spacer. In case of Fig 13, it has been depicted that the effect of nanocomposite sidewall spacer dielectric film on the threshold voltage of MOSFET degradation in short-channel performance associated with high-K_{sp} dielectrics. Thus, it is cleared that replacement of Si₃N₄ with PTFE/SiO₂ leads to a significant degradation of the threshold voltage of MOSFET.

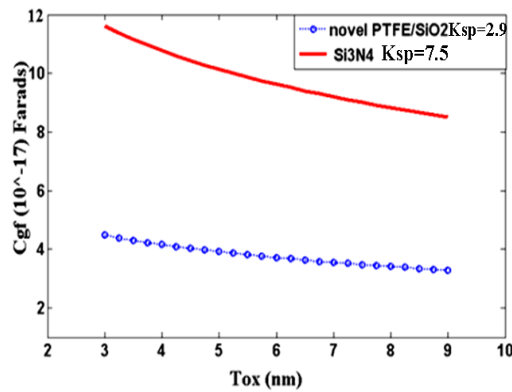


Figure 10. Effect of Gate oxide thickness T_{ox} of nanocomposite side-wall spacer dielectric film gate in electrode fringing capacitance C_{gf} using PTFE/SiO₂ and Si₃N₄ spacer K_{sp}

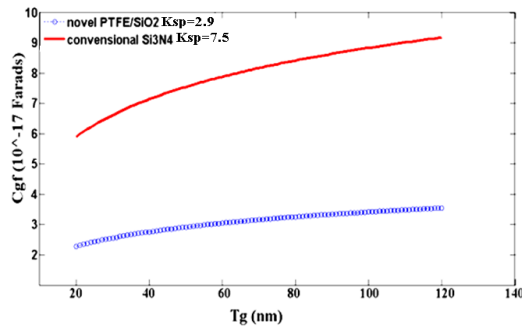


Figure 11. Effect of Gate electrode thickness T_g of nanocomposite side-wall spacer dielectric film gate in electrode fringing capacitance C_{gf} using PTFE/SiO₂ and Si₃N₄ spacer K_{sp}

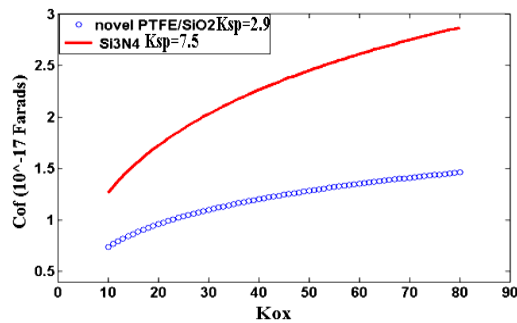


Figure 12. Effect of gate oxide thickness T_{ox} in gate dielectric fringing-capacitance C_{of} with PTFE/SiO₂ and Si₃N₄

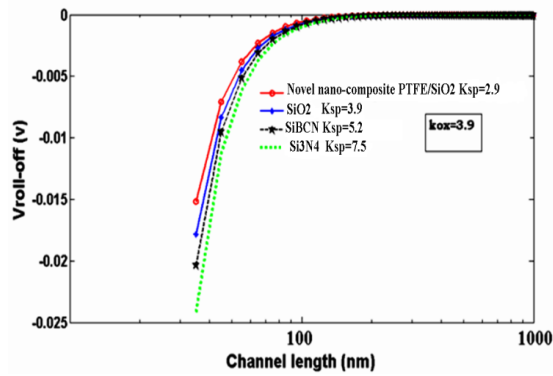


Figure 13. Influence of K_{sp} value of sidewall spacer on the threshold voltage of MOSFET

3.3. Modification of Enhancing TFTs using High-K and Low-K Gate Sidewall Spacer with Nanocomposite Materials

Figure 14 shows the effect of both novel nanocomposite gate and spacer dielectric film in internal fringe capacitance C_{bottom} . Figure 14 shows the variation of internal fringing capacitance as a function of normalized gate length for both novel nanocomposite gate dielectric K_{ox} PVP/La₂O₃ and gate spacer K_{sp} PTFE/SiO₂, with conventional gate dielectrics and gate sidewall spacer dielectric film. This figure shows the fringing capacitance C_{bottom} decreases with increasing the gate length but the using of novel nanocomposites give the highest bottom fringing capacitance over conventional materials.

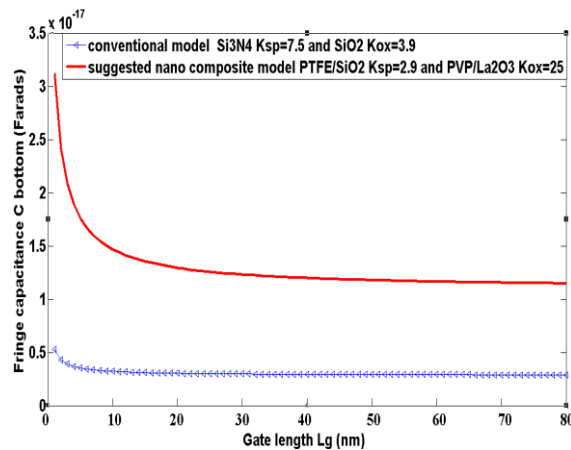


Figure 14. Effect of gate length L_g on internal fringing-capacitance C_{bottom} using novel nanocomposite PVP/La₂O₃ as gate dielectric K_{ox} and PTFE/SiO₂ gate sidewall spacer dielectric film K_{sp}

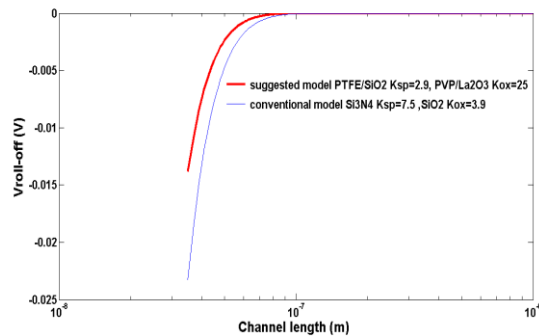


Figure 15. Influence of novel nanocomposite K_{ox} and K_{sp} on the threshold voltage of MOSFET

Figure 15 shows the effect of both novel nanocomposite gate and spacer dielectric film in the threshold voltage of MOSFET. It has been cleared that, the threshold voltage roll-off decreases more with using of novel nanocomposite gate dielectric K_{ox} PVP/La₂O₃ and gate spacer K_{sp} PTFE/SiO₂ than the conventional material which used in the short-channel region of <100 nm because the FIBL effect is enhanced for large K_{sp} values. Therefore, low- K_{sp} sidewall spacer can alleviate the FIBL effect, especially for nano MOSFET

4. CONCLUSIONS

Highly accurate analytical models have been provided for fringing field effects with the impact of using nanocomposite PVP/La₂O₃ high-K gate dielectrics on device short channel and circuit performance. Novel nanocomposite PTFE/SiO₂ low-K sidewalls spacer has been improved the device short channel performance by reducing the gate fringing field effect. Novel nanocomposite high-K gate dielectric material PVP/La₂O₃ has been improved the performance of TFT devices by increasing the surface potential and decreasing the threshold voltage. High permittivity's K_{ox} gate dielectric and greater physical thicknesses, a factor of K_{ox}/K_{SiO_2} prevent direct gate tunneling and decreasing gate leakage current.

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