

A Novel Analysis of Improving Displacement Factor Using IVDFC in Distribution Systems

M. Padmarasan, C. T. Manikandan, N.Karthikeyan, L. Jayaprakash, C. S. Ajin Sekhar
Department of EEE, Panimalar Institute of Technology, Chennai, India

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ABSTRACT

In this paper discuss the new approach for improving displacement factor using an Interline Dynamic Voltage Restoring and Displacement Factor Controlling Device (IVDFC) in a distribution system. An Interline Dynamic Voltage Restorer (IDVR) is perpetually engaged in distribution systems to mitigate voltage sag/swell problems. An IDVR simply consists of numerous dynamic voltage restorers (DVRs) sharing a common dc link connecting independent feeders to safe electric power to critical loads. The IDVR is operated that it hold the voltage across the critical load bus terminals constant at system nominal frequency irrespective of the changes occurring in source voltages frequency. While one of the DVRs compensates for the local voltage sag in its feeder, the other DVRs reload the common dc-link voltage. For normal voltage levels, the DVRs should be bypassed. Instead of bypassing the DVRs in normal conditions, this paper proposes operating the DVRs, if needed, to improve the displacement factor (DF) of one of the involved feeders. DF improvement can be achieved via active and reactive power exchange (PQ sharing) between different feeders. To successfully apply this concept, several constraints are addressed throughout the paper. The simulation model for this system is developed using MATLAB which is shown that the voltage across the critical load is regulated completely.

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Corresponding Author:

M.Padmarasan
Department of Electrical and Electronics Engineering,
Panimalar Institute of Technology, Chennai, India.
Email: padmaras_mathi@yahoo.com

1. INTRODUCTION

Power Quality (PQ) measures a wide range of power supply characteristics which can influence the performance of equipment and processes. Many PQ characteristics are a function of both the supply system and end-user system and equipment characteristics. The PQ characteristics [1-2] can be classified into two major types: steady-state PQ variations and disturbances. The inclusion of the steady-state PQ characteristics of the supply voltage are frequency variations, voltage variations, voltage fluctuations, unbalance in the three-phase voltages, flicker and harmonic distortion. In modern power systems many devices such as power electronic equipment and arc furnaces, etc creates harmonics and noise.

Power frequency variations are defined as the deviation of the power system fundamental frequency from its specified nominal value (e.g., 50 or 60 Hz) [3-4]. The frequency deviation duration range can between several cycles to several hours. These variations are usually caused by fast changes in the loads connected to the system. The maximum tolerable variation in supply frequency is often limited within ± 0.5 Hz. Voltage notching can sometimes be mistaken for frequency deviation. The notches may come sufficiently close to zero to cause errors in instruments and control systems that rely on zero crossings to derive frequency or time.

The well-known convention power devices such as Distribution STATCOM (DSTATCOM), Interline Dynamic Voltage Restorer (IDVR) and Unified Power Quality Conditioner (UPQC) are available

for protection of a critical load from disturbances occurring in the distribution system [4]. The disturbances may be due to voltage unbalance, sag/swell, distortion etc. The frequency variation is also one of the major PQ problems.

This paper discusses the improvement of displacement factor of a critical load bus using an interline dynamic voltage restorer (IDVR). The critical load requires a balanced sinusoidal waveform across its terminals at system nominal frequency of 50/60 Hz. It is assumed that the frequency of the supply voltages is varying or is different from the system nominal frequency. An IDVR is a power electronic controller and is realized using voltage source converters (VSCs). It injects three independent single-phase voltages in the distribution feeder such that the load voltage is perfectly regulated at system nominal frequency. In general, the DVR is operated in such a fashion that it does not supply or absorb any real power during the steady-state operation [5]. The dc link of the VSCs is supplied through a dc capacitor/ dc source. The capability of a DVR to regulate the voltage of a critical load depends on the energy stored in the dc link. In case of a frequency mismatch, the total real power requirement of the load has to be supplied through the DVR. To provide this real power, the dc link of the DVR must be supplied from the distribution feeder itself. The two DVRs in different feeders are connected to common dc link energy storage. One DVR can reload energy to the dc link to maintain the dc link voltage at a specific level while other DVR carries out voltage regulation during sags.

Distribution networks are mostly inductive at the fundamental frequency because of the nature of the prevailing connected loads (e.g., induction motors). This reduces the displacement factor (DF) and places an additional burden on the electrical supply. Low DF operation is not suggested due to several negative effects on the power system including:

- 1) higher current for a given active power and a corresponding increase in total copper loss (i.e., system efficiency decrease);
- 2) lower utilization of power system components;
- 3) voltage regulation issues and rising power delivery costs.

Several practical techniques are commonly used to improve DF [6]. DF improvement employing capacitor banks with size and location optimization has been introduced [7]. The optimal location and size of the capacitor bank to be placed in radial distribution feeders to improve their voltage profile and to reduce the total energy loss are presented [8]. Different techniques are employed to decrease the power loss in distribution networks. In the feeder reconfiguration concept in distribution systems is introduced to decrease system loss. In a combined system for harmonic suppression and reactive power compensation is proposed not only to improve the DF but also the power factor.

A STATCOM can be used as a feasible choice for DF improvement. Suitable modification of the phase and magnitude of the STATCOM output voltages facilitate effective control of active as well as reactive power exchanges between the STATCOM and the distribution system. Such a configuration allows the device to absorb or generate controllable active and reactive powers. A STATCOM has various features, including fast response, low-space requirement, and good stability margins. Recently, it is rapidly replacing the conventional naturally commutated reactive power controllers and static VAR compensators [9].

The reactive power supplied by the STATCOM for DF improvement is capacitive in nature. Instinctively, the higher the STATCOM's reactive power, the higher the dc-link voltage of the STATCOM (the higher the voltage requirements of the semiconductor devices).

The DVR is one of the most common and effective solutions for protecting critical load against voltage sags [10] [11]. The DVR is a power electronic device used to inject three-phase voltages in series and in synchronism with the distribution feeder voltages in order to compensate for voltage sags. Moreover, it can be efficiently used to augment the fault ride through capability in wind applications. Detection time is an important factor in the voltage restitution process. Fast detection algorithms and effective control schemes for a DVR are proposed respectively. Space vector modulation (SVM) is the suggested modulation scheme in a DVR due to its simple digital realization and improved dc-link utilization. In distribution systems, load voltage restoration can be achieved by injecting active and/or reactive power into the distribution feeder. Active power capability of the DVR is governed by the capacity of the energy storage element and the engaged compensation technique. Several control techniques have been proposed for voltage sag compensation, such as presag, in-phase, and minimal energy control approaches [12].

2. CONVENTIONAL METHOD

If the required power for voltage restoration is obtained from the neighboring feeder(s), the compensating device is technically called an interline dynamic voltage restorer (IDVR) [13]. The basic concept behind the IDVR is derived from the interline power flow controller (IPFC) proposed by Gyugyi in 1999 [14] to exchange power between parallel transmission lines. The two converters of the IPFC shown in Figure 1 are used to control the transmitted power in each line (P1 and P2) and active power transfer between

lines (P12). With respect to the line current, the injected voltage has two components. The quadrature component provides reactive power compensation for the line, while the in-phase component absorbs or generates the required active power.

The main differences between an IPFC, IDVR, and the proposed system are given in Table I. In this table, the IPFC, which is used in transmission applications, is compared with an IDVR and IVDFC, which are considered for distribution systems. It should be noted that the IPFC was the inspiration for proposing the IDVR for distribution networks. The IDVR can be used to mitigate voltage sag, or swell, at critical loads in distribution systems. It consists of several back-to-back voltage source converters with common dc link connecting independent feeders as shown in Figure 2.

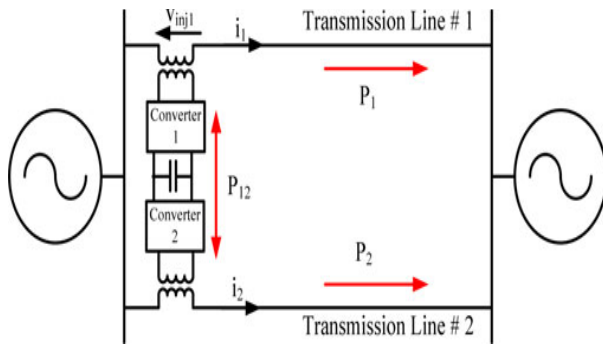


Figure 1. Single Line Diagram of an IPFC in Transmission System

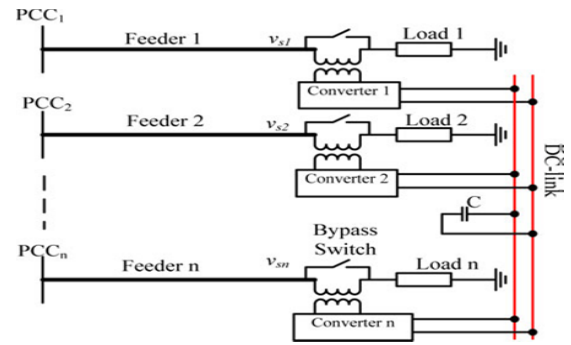


Figure 2. Single Line Diagram of Multiline IDVR in the Distribution System

Table 1. Salient Features of the IPFC, IDVR and IVDFC

	IPFC	IDVR	IVDFC (Proposed concept)
Function	It is used in transmission systems to control the power flow of parallel transmission lines.	It is used in distribution systems for voltage sag/swell restoration.	It is used in distribution systems for voltage sag/swell restoration and improvement of displacement power factor during normal conditions.
Operation	Employed in normal operation	Employed in abnormal conditions	It can be employed in normal as well as abnormal conditions
In-phase voltage injection	Active power control	When the feeder is switched to power control mode, the in-phase voltage component represents the active power to be pumped/ absorbed by that feeder to/from the DC-link (Active power control).	When the feeder is switched to power control mode or DF improvement mode, the in-phase voltage component represents the active power to be pumped/ absorbed by that feeder to/from the DC-link (Active power control).
Quadrature voltage injection	Line reactive impedance control	When the feeder is switched to power control mode, the quadrature voltage component is used to keep the load voltage magnitude of that feeder constant (load voltage control).	When the feeder is switched to power control mode or DF improvement mode, the quadrature voltage component is used to keep the load voltage magnitude of that feeder constant (load voltage control).

Each converter can be operated in either power control (PC) or voltage control (VC) modes. If one of the feeders is subjected to voltage sag, its converter will operate in VC mode and the required power for voltage restoration will be absorbed from the dc link. In this state, the other converters connected to the healthy feeders should be switched to PC mode to replenish the dc-link voltage; a power-sharing scheme to determine the reference power of each healthy feeder is presented [15].

The injected voltage in a healthy feeder during PC mode should have two components. The first component is in-phase with line current, which absorbs active power from the supply and provides it to the dc link to support its voltage. The second component is in quadrature with the line current and is used to avoid load voltage magnitude perturbations after voltage injection.

Drawbacks of the Conventional method are:

- 1) System efficiency decrease
- 2) Total Copper loss increase
- 3) voltage regulation issues and
- 4) Rising power delivery costs.

3. PROPOSED METHOD

During normal operating conditions (i.e., all feeders are healthy), the DVRs are typically bypassed via bypass switches, or they can be alternatively used for load sharing purposes as presented [16]. Instead of bypassing the IDVR in normal operation, this paper proposes a new operational mode, namely PQ sharing mode, to improve the DF of one of the involved feeders by sharing active and reactive power among different system feeders through the buffering stage (the common dc link). To apply this concept, several constraints are observed throughout the paper. The proposed interline dynamic voltage restoring and DF controlling device (IVDFC) is supported using simulation and experimental results.

Similar to the IDVR, the two-line IVDFC simply consists of two voltage source converters connected back-to-back with a common dc link as shown in Figure 3. For normal voltage levels, achieving active power exchange P_{ex} between the feeders (from sourcing feeder to receiving feeder), requires controlled voltage injection in each feeder by the corresponding converter. This injected voltage should not perturb the load voltage magnitude of both feeders; therefore, both converters are operating under PC mode.

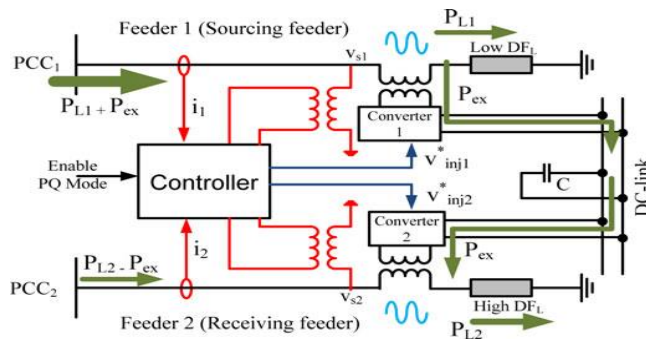


Figure 3. Principle of IVDFC System Operation During Normal Conditions (PQ Sharing Mode)

3.1. Sourcing Feeder

The converter in the sourcing feeder is responsible for feeding energy into the dc link via injecting a controlled voltage (magnitude and phase) through the series coupled transformer allowing for power exchange. In this paper, in order to emulate the effect of voltage injection on the feeder DF, the injected voltage is emulated using a voltage drop across a series virtual impedance as shown in Figure 4(a) [17] [18]. The resistive component of this virtual impedance absorbs active power (P_{ex}) from the source, while the function of the capacitive reactance component is to maintain a constant load voltage magnitude. After voltage injection, the supply's active power increases while its reactive power decreases due to the virtual injected capacitive reactance, hence, the sourcing feeder DF eventually increases.

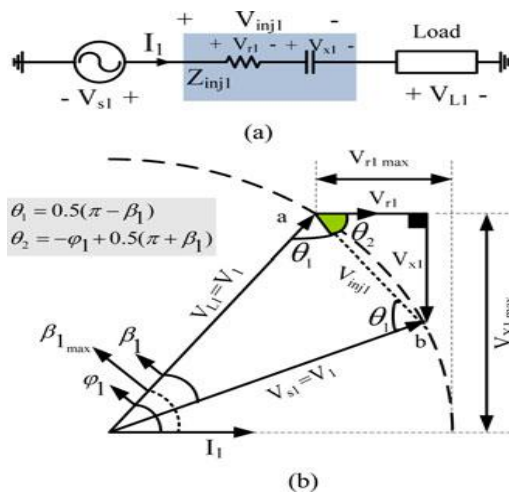


Figure 4. Sourcing Feeder: (a) Per-Phase Equivalent Circuit with Virtual Impedance Injection and (b) Corresponding Phasor Diagram

Assuming a three-phase balanced load is connected to the feeder; the per-phase equivalent circuit of the feeder with series virtual impedance injection is shown in Figure 4(a), while the corresponding phasor diagram is shown in Figure 4(b).

For a given transferred active power P_{ex} (through dc link), the load power is

$$PL1=3I1V1DFL1=3I1V1 \cos \phi1 \tag{1}$$

The supplied power is

$$Ps1=PL1+P_{ex}=3I1V1 \cos(\phi1-\beta1) \tag{2}$$

Where P_{ex} is the power absorbed from the source and pumped into the dc link.

From (2), the angle $\beta1$ can be obtained as follows:

$$\beta1= \phi1-\cos^{-1}((PL1+P_{ex})/3I1V1) \tag{3}$$

The maximum allowable P_{ex} corresponds to unity input DF. For a given load DF, the maximum P_{ex} is

$$P_{exmax}=3I1V1 (1-DFL1) \tag{4}$$

The virtual injected resistance $r1$, which represents absorbed active power from sourcing feeder, is

$$r1=P_{ex}/3I1^2 \tag{5}$$

From the phasor diagram shown in Figure 4(b), the virtual injected capacitive reactance $x1$ is

$$x1=r1 \tan (-\phi1 + (\pi + \beta1)/2) \tag{6}$$

For any amount of desired exchanged active power (P_{ex}) and load-side parameters ($I1$, $V1$, and $DFL1$), the voltage source converter at the sourcing feeder injects this power to the dc link without affecting load voltage magnitude by supplying a voltage of magnitude $2V1 \sin (\beta1/2)$. This voltage's phase angle lags the supply voltage phase angle by $(\pi - \beta1) /2$, as shown in Figure 4(b).

3.2. Receiving Feeder

The converter in the receiving feeder is responsible for absorbing the transmitted power from the sourcing feeder via voltage injection; hence, the power controller has a power command of $-P_{ex}$. The injected voltage in this case is equivalent to injecting a virtual negative resistance $-r2$ in series with an inductive reactance $x2$, as shown in Figure 5(a).

From the equivalent circuit and the phasor diagram shown in Figure 5(a) and (b), the angle $\beta2$ is

$$\beta2=-\phi2 +\cos^{-1}((P_{L2}-P_{ex})/3I2V2) \dots \tag{7}$$

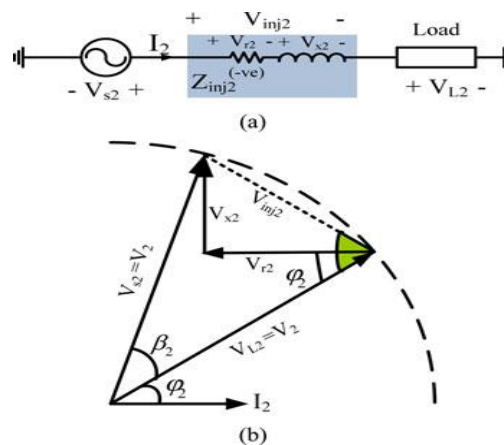


Figure 5. Receiving Feeder: (a) Per-phase Circuit with Virtual Impedance Injection and (B) Corresponding Phasor Diagram

To absorb this amount of transferred active power without affecting the load voltage magnitude, the injected voltage in the receiving feeder should have a magnitude of $2V_2 \sin(\beta_2/2)$, and its phase angle leads the supply voltage phase angle by $(\pi - \beta_2)/2$. It is worth noting that the supply's active power decreases while its reactive power increases due to the virtual injected inductive reactance, i.e., the receiving feeder DF eventually decreases.

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3.3. PQ Sharing Mode for DF Improvement During Normal Operation

The operating mode presented in this subsection will be illustrated using a two-line IVDFC, where feeder 1 is feeding a load with a low lagging DF DF_{L1} , while feeder 2 is feeding a load with a high lagging DF DF_{L2} . Since feeder 1 DF is lower than feeder 2 DF, it will be the sourcing feeder, while feeder 2 will be the receiving feeder. When applying the proposed PQ sharing mode, the sourcing feeder DF will be improved, while the receiving feeder DF decreases. As a general constraint, the new receiving feeder DF should be greater than a certain acceptable limit DF_a imposed by the utility company to avoid additional fees. A typical limit of 0.95 is usually employed in distribution networks [19]. Figure 6 is used to explain the proposed sharing mode.

With PQ sharing mode disabled, the DF at the PCC for each feeder is equal its load DF. If a certain amount of active power P_{ex} is transferred from feeder 1 to feeder 2, such that its DF reaches a certain desired value DF_d , as shown in Figure 7(a), the DF of feeder 2 will be reduced, as depicted by Figure 6(b).

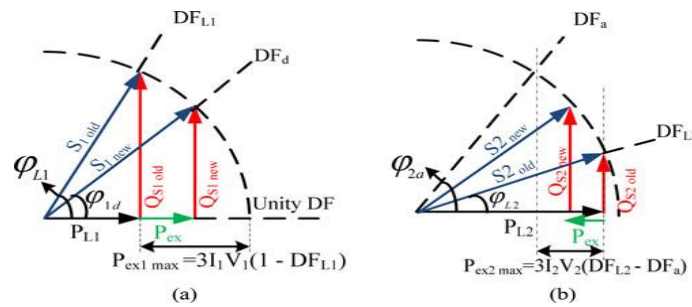


Figure 6. Effect of PQ Sharing Mode on (a) Feeder1 and (b) Feeder 2

The sourcing feeder DF can be improved to DF_d , if and only if, the needed active power P_{ex} to achieve this condition is less than the needed power to decrease the receiving feeder's DF to the accepted DF limit DF_a . If this condition is not satisfied, the DF of the sourcing feeder will be improved, but it will not reach the desired level, and the receiving feeder DF will be limited to its acceptable level. Hence, the reference active power (P_{ex}) during PQ sharing mode is

$$P_{ex} = \min [3I_1V_1 (DF_d - DFL1) , 3I_2V_2 (DFL2 - DF_a)] \tag{8}$$

This rule is defined as the minimum of two terms; the first term gives the needed increment in sourcing feeder supplied active power to improve its DF to a desired level DF_d , while the second term gives the needed decrement in receiving feeder supplied active power to reduce its DF to the accepted value DF_a . If the receiving feeder's active power is higher than that of the sourcing feeder, a slight variation in its DF introduces a noticeable improvement in sourcing feeder DF. Generally, the DF improvement will reduce the magnitude of currents in the up-stream branches of the grid, i.e., decrease grid losses.

It has to be noted that, in the proposed method, the DF is improved by reducing the difference between supply voltage and current phase angles assuming a constant volt-ampere condition. As a result, the employment of PQ sharing mode will not affect the feeder losses since the current magnitudes are kept constant, but converters losses will be added to the feeder losses to represent the total losses of the system (from points of common coupling to load feeding points).

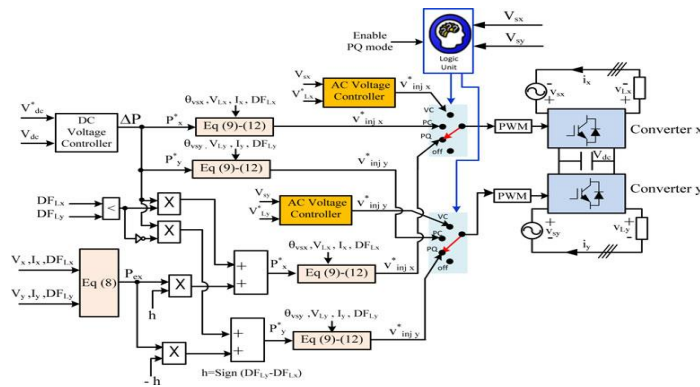


Figure 7. Proposed Controller

Figure 7 shows the proposed controller for a two-line IVDFC (two feeders are involved, namely, feeder *x* and feeder *y*), which is able to manage the power transfer through the dc-link in normal as well as abnormal operating conditions. As a general controller, voltage sag/swell and DF improvement problems are merged into one control circuit. Referring to Figure 8, each converter may be switched to one of four possible modes (off mode, VC mode, PC mode, or *PQ* mode). The PCC voltages are continuously monitored by a logic unit that is responsible for choosing the appropriate mode of operation for each converter based on the voltage levels.

The following section will show how different modes of operation are handled individually in the proposed controller. A set of scenarios can be envisioned for the system. The main cases are summarized in Table II and in the following subsections (where the hyphenated condition describes the state of one of the feeders to the left of the hyphen and the other feeder to the right of the hyphen). For all other cases, the converters will be switched to the off position.

A. Normal–Normal (PQ Sharing Mode is Disabled)

In this case, the logic unit selects the off positions (see Figure 7) for both converters.

B. Normal–Normal (PQ Sharing Mode is Enabled)

In this case, the logic unit selects the *PQ* positions (see Figure 7) for both converters after verifying all constraints that accompany this mode. Based on the DFs of the loads connected to the involved feeders (*DFL_x* and *DFL_y*), the direction of active power flow will be defined. The feeder with a lower load DF will be the sourcing feeder with a positive active power reference, and the other feeder will be the receiving feeder with a negative active power reference. In Figure 8, the sign of the variable *h*, which represents the difference between the two DFs, is used to determine the sign of the different reference powers.

To maintain a constant dc-link voltage during the *PQ* sharing mode, the output of the dc link voltage controller, ΔP (which represents the active power needed to regulate the dc link) is added to the reference active power of the sourcing feeder. To achieve that, the two DFs (*DFL_x*, and *DFL_y*) are compared to decide the sourcing and receiving feeders. The comparator output is used to add ΔP to the reference active power of the sourcing feeder only as shown in Figure 7.

Table 2. Proposed Controller Combinations

Parameter	Value
Bus 1 and Bus 2 Voltage	220∠0 V (rms)
Load (A) impedance	<ul style="list-style-type: none"> Normal conditions Case1: 40 Ω, 0.8 DF lag Case 2: 40 Ω, 0.5 DF lag Voltage sag condition 40 Ω, 0.8 DF lag
Load (B) impedance (critical load)	40 Ω, 0.99 DF lag
Load (C) impedance	13.33 Ω, 0.99 DF lag
<i>DF_d</i> for bus 1	0.95 Lag
<i>DF_a</i>	0.95 lag

C. Normal–Voltage Sag

If one feeder exhibits voltage sag, the logic unit has to switch its series converter to VC position (see Figure 8) to regulate the load voltage, and the required power for restoration will be absorbed from the dc link. The converter of the healthy feeder will be switched to its PC position (see Figure 8) to replenish the dc-link voltage. The needed power to restore the dc link voltage will be the output of the dc voltage controller. This power is used to estimate the corresponding converter reference voltage.

D. Normal–Voltage Swell

If one feeder exhibits voltage swell, the logic unit switches its series converter to the VC position (see Figure 8) to regulate the load voltage. Additional power is then fed to the dc link. The converter of the healthy feeder will be switched to its PC position (see Figure 8), to avoid increasing the dc-link voltage. The amount of power, which should be absorbed by the healthy feeder, will be the output of the dc voltage controller.

4. SIMULATION

A simulation model for two independent buses is built using MATLAB/SIMULINK as in Figure 8.

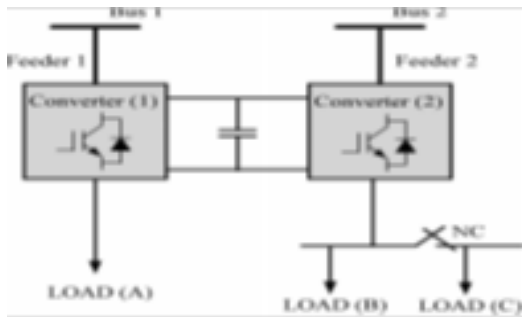


Figure 8. Two-Line IVDFC System

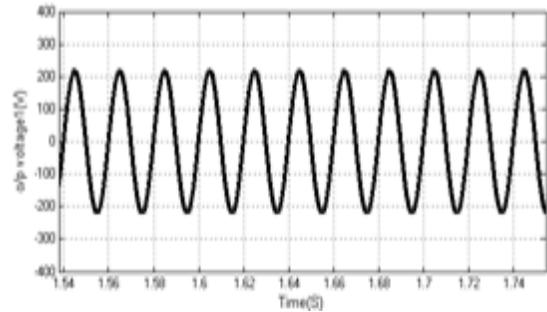


Figure 9. Output Voltage of Healthy Line

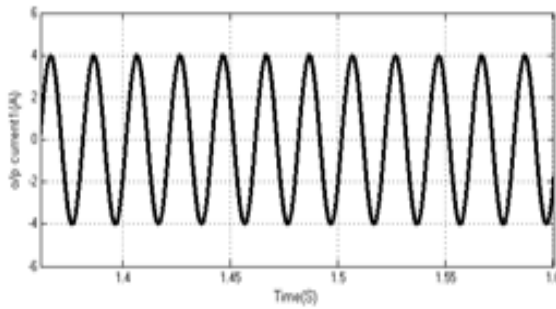


Figure 10. Output Current of Healthy Line

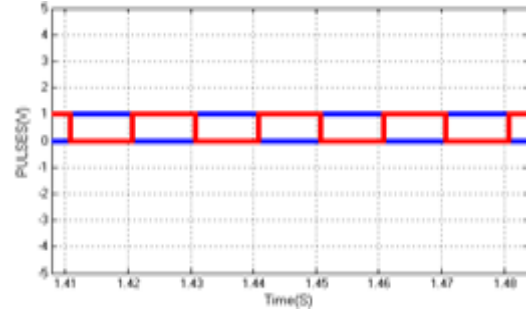


Figure 11. Gate Pulses of IVDR

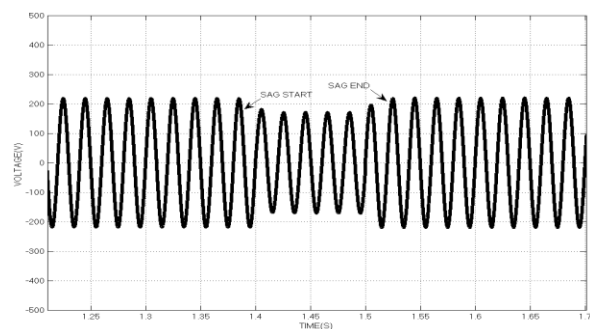
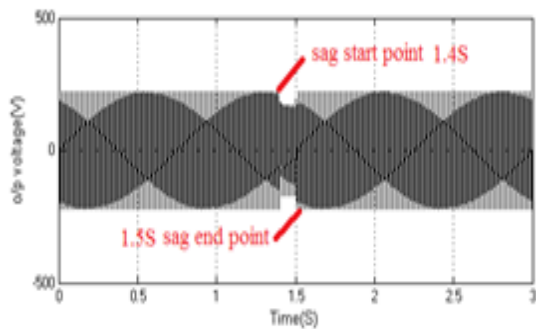


Figure 12. Output Voltage of IVDR

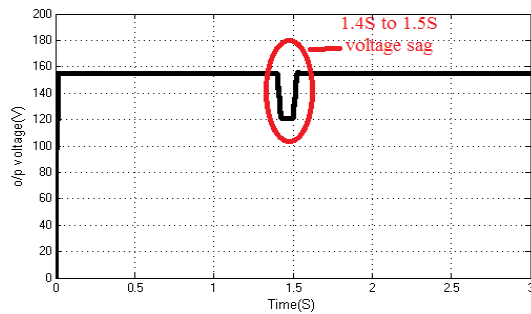


Figure 13. Output Voltage Under Sag Condition

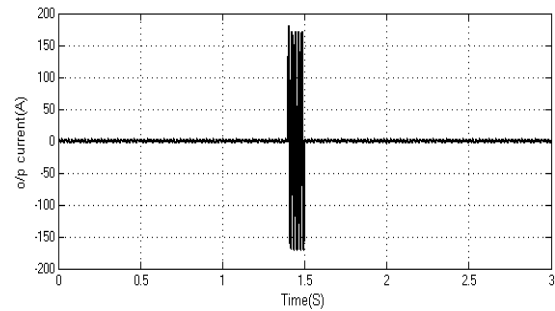


Figure 14. Rms Output Voltage of IVDR

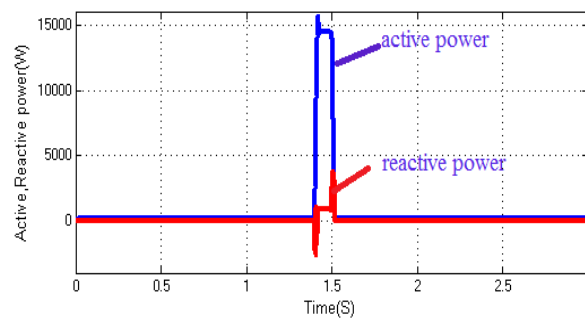


Figure 15. Output Current

Figure 16. Power Quality of IVDR

5. CONCLUSION

This paper proposes a new operational mode for the IDVR to improve the DF of different feeders under normal operation. In this mode, the DF of one of the feeders is improved via active and reactive power exchange between feeders through the common dc link. The main conclusions of this work can be summarized as follows:

- Under PQ sharing mode, the injected voltage in any feeder does not affect its load voltage/current magnitude, however, it affects the DFs of both sourcing and receiving feeders. The DF of the sourcing feeder increases while the DF of the receiving feeder decreases.
- When applying the proposed concept, some constraints should be satisfied to maintain the DF of both sourcing and receiving feeders within acceptable limits imposed by the utility companies. These operational constraints have been identified and considered.
- The proposed mode is highly beneficial if the active power rating of the receiving feeder is higher than the sourcing feeder. In this case, the DF of the sourcing feeder will have a notable improvement with only a slight variation in DF of the receiving feeder. The proposed concept has been supported with simulation and experimental results.

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